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Hafnium Dioxide Gate Dielectrics, Metal Gate Electrodes, and Phenomena Occurring at their Interfaces

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by

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Hafnium Dioxide Gate Dielectrics, Metal Gate Electrodes, and Phenomena Occurring at their Interfaces

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As metal-oxide-semiconductor field-effect transistor (MOSFET) gate lengths scale down below 45 nm, the gate oxide thickness approaches 1 nm equivalent oxide thickness. At this thickness, conventional silicon dioxide (SiO_2) gate dielectrics suffer from excessive gate leakage. Higher permittivity dielectrics are required to counter the increase in gate leakage. Hafnium dioxide (HfO_2) has emerged as a promising dielectric candidate. HfO_2 films deposited using metal organic chemical vapor deposition are being studied to determine the impact of process and annealing conditions on the physical and electrical properties of the gate dielectric. This study indicates that deposition and annealing temperatures influence the microstructure, density, impurity concentration, chemical environment of the impurities, and band-gap of the HfO_2 dielectric. Correlations of the electrical and physical properties of the films indicate that impurities in the form of segregated carbon clusters, and low HfO_2 density are detrimental to the leakage properties of the gate dielectric.

Additionally, as the HfO_2 thickness scales, the additional series capacitance due to poly-silicon depletion plays a larger roll in reducing the total gate capacitance. To solve this problem, high performance bulk MOSFETs will require dual metal gate electrodes possessing work functions near the silicon band edges for optimized drive current. This investigation evaluates TiN, Ta-Si-N, Ti-Al-N, WN, TaN, TaSi, Ir and IrO_2 electrodes as candidate electrodes on HfO_2 dielectrics. The metal-dielectric compatibility was studied by annealing the gate stacks at different temperatures. The physical stability and effective work functions of metal electrodes on HfO_2 are discussed.

Finally, Fermi level pinning of the metal is a barrier to identifying materials with appropriate threshold voltages. The contributions to the Fermi level pinning of platinum electrodes on HfO_2 gate dielectrics are investigated by examining the impact of oxygen and forming gas anneals on the effective work function of platinum-HfO_2-silicon capacitors. Oxygen anneals result in higher effective work functions for platinum on HfO_2 than forming gas anneals. The presence of interfacial oxygen vacancies or Pt-Hf bonds is believed to be responsible for a degree of pinning that is stronger than predicted from the metal induced gap states model alone.

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Chapter 1: Introduction

1.1 OVERVIEW

Recent technological limits to the shrinking of silicon-based integrated circuits require the implementation of new materials into the core of the transistor. To satisfy the need for faster, more functional, and cheaper integrated circuits, the silicon-based microelectronics industry has scaled the dimensions of devices on integrated circuits, effectively building microchips with more devices per unit area. It was predicted by Gordon Moore in 1965, in what is now termed "Moore's Law," that the number of components on a chip would double every 18 months. Amazingly, this dramatic rate of miniaturization has been achieved every year since then with only evolutionary changes to the materials used to build the transistors.

The traditional metal-oxide-semiconductor field effect transistor (MOSFET) is a four-terminal electronic device (Fig. 1.1). Two of the four terminals comprise a MOS capacitor (MOSCAP) structure that consists of a gate electrode, an insulating dielectric layer, and the silicon substrate. When a bias is applied to the gate electrode an electric field is produced across the dielectric layer. The electric field induces an opposite charge at the surface of the silicon substrate. The presence of these charges results in a conductive channel between the source and drain region of the MOSFET. Thus, the bias applied to the gate electrode controls whether the current between the source and the drain is ON or OFF. Historically, the materials used in a MOSFET include a heavily doped polycrystalline silicon (poly-silicon) gate electrode, a silicon dioxide (SiO_2) gate dielectric, and heavily doped regions in the silicon substrate formed by ion implantation

that comprise the source and the drain regions. The ion implanted dopant atoms in the electrode, source, and drain are typically phosphorous or arsenic for a device where the charge carriers are electrons (or NMOSFET) and boron for a device where the charge carriers are holes (or PMOSFET).

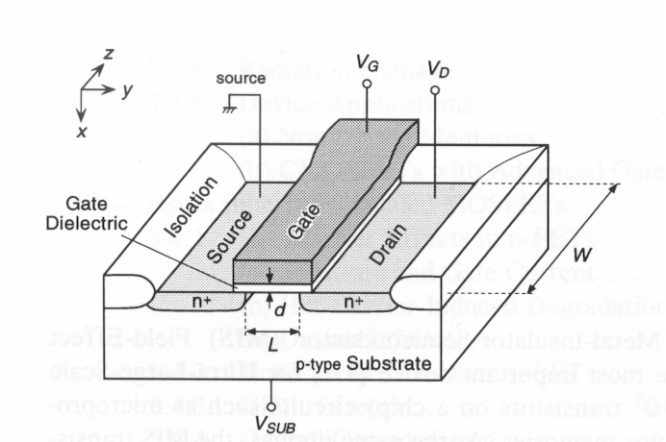

Figure 1.1: Cross-section of an n-channel metal oxide semiconductor (NMOS) transistor.

In transistor operation, applying a bias to the gate electrode produces an electric field across the capacitor structure. This electric field modulates the carrier concentration in the channel and therefore controls the flow of current from the source to the drain. Enhanced MOSFET performance can be achieved by scaling or shrinking the device dimensions.[1] The scaling process results in faster switching speeds, lower power dissipation, and smaller device and circuit areas. Ultimately, this provides the consumer with faster circuit performance, reduced energy consumption or longer battery lifetime, and a reduced cost integrated circuit.

From a transistor perspective, increased switching response times are achieved by increasing the drain current of a transistor. The drain current in saturation ($I_{D,sat}$) is approximated by

$$(1)\ I_{D,sat} = \frac{\overline{\mu}_n Z C_{inv}}{2L}(V_G - V_T)^2$$

where Z is the width of the transistor, L is the channel length, $\overline{\mu}_n$ is the channel carrier mobility, C_{inv} is the capacitance density of the MOSFET when it is in inversion, V_G is the voltage applied to the gate of the device, and V_T is the threshold voltage of the device.[2] It can be seen from this equation that either a reduction in the channel length (L) or an increase in the capacitance (C_{inv}) will increase the drain current per unit width. The primary component of C_{inv} is the capacitance of the oxide layer given by

$$(2)\ C_i = \frac{\kappa \varepsilon_0 A}{t}$$

where C_i is the oxide capacitance, A is the capacitor area, κ is the dielectric constant, or relative permittivity, ε_0 is the permittivity of free space, and t is the thickness of the dielectric. It is observed that C_i can be increased by reducing the thickness (t) of the SiO_2 dielectric. However, a limit to the thickness scaling of the SiO_2 dielectric is rapidly being approached.

This limit is predicted to occur when the smallest feature widths on a microprocessor approach 65nm. At this dimension the SiO_2 gate dielectric will thin to below 13 Å. At 13 Å the dielectric material will only have a bulk thickness of three atomic layers of silicon.[3,4] Around this thickness, electrical leakage current through the dielectric becomes excessive and is expected to cause problems due to either high power dissipation or circuit reliability.[5] One solution to this problem is to replace SiO_2 dielectrics with higher permittivity dielectrics. A dielectric with a higher permittivity (κ) can be thicker and still achieve the same or greater capacitance as a thinner SiO_2 dielectric ($\kappa = 3.9$).

However, as will be discussed later, replacing SiO_2 with a high-κ gate dielectric is not trivial. The high quality SiO_2 gate dielectric grown by thermal oxidation of the silicon substrate is precisely the reason why silicon has been the preferred semiconductor substrate for integrated circuit manufacturing. Thermally grown SiO_2 dielectrics result in interfaces with the silicon substrate that possess an exceptionally low number of electronically active defects ($\sim 10^{10}/cm^2$). In fact, the SiO_2 gate dielectrics are practically so perfect that their only disadvantage is their low dielectric constant. This dissertation will explore the film growth and materials properties of a high permittivity gate dielectric.

Since increasing the gate capacitance is required for increasing MOSFET drive current, device scaling mandates a consideration of other factors that degrade the total

inversion capacitance. When a MOSFET is operated in inversion there are actually two additional capacitances in series with the oxide capacitance. Taking these factors into consideration the total capacitance is given by

$$(3)\ \frac{1}{C_{inv}} = \frac{1}{C_{sub}} + \frac{1}{C_i} + \frac{1}{C_{poly}}$$

where C_i is the aforementioned oxide capacitance, C_{sub} is a capacitance due to quantum mechanical effects which force the centroid of inversion charge in the substrate to be a few Ångstroms away from the Si/SiO_2 interface, and C_{poly} is due to a gradual potential drop, or band bending, in the poly-Si gate electrode (Fig. 1.2). Further discussion on the origins of the C_{sub} is beyond the scope of this dissertation, but detailed discussions are available.[1,6]

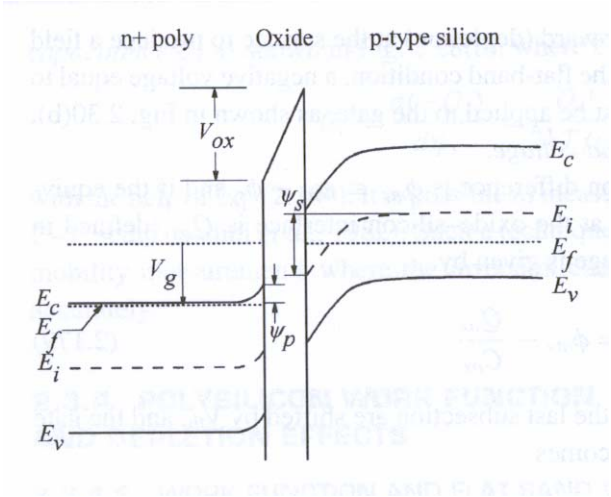

Figure 1.2: Schematic band diagram of n+ poly-Si/oxide/p-type silicon. Poly-silicon depletion is indicated by the slight band bending in the n+ poly near the oxide interface.

The C_{poly} contribution, which is frequently referred to as poly-silicon depletion, is a result of the sum of inversion and depletion charges in the substrate being greater than the impurity density (N_{poly}) near the poly-Si - oxide interface. Since charge neutrality requires that the field lines for every carrier in the substrate are screened by a carrier in the electrode, the field lines from the substrate penetrate a finite distance into the poly-Si electrode before encountering enough carriers to cancel the sum of their electric fields. The screening of charge over a finite distance into the poly-Si is the origin of the gradual potential drop and band bending in the poly-Si electrode.

When the oxide thickness is large, the contribution of C_{sub} and C_{poly} towards degrading the total capacitance is small. However, for scaled devices, the series capacitances from poly-depletion and quantum effects in the substrate can significantly degrade the total capacitance. This can be illustrated by neglecting any contribution of C_{sub} to the inversion capacitance and examining the following equations. Since charge neutrality requires that the depletion charge in the poly-Si equals the sum of the inversion charge and the depletion charge in the silicon, the depletion charge is given by

$$(4)\ Q_{poly} = qN_{poly}W_{poly} = Q_{inv} + Q_{dep} = C_i\left|V_{G'}\right| + (2\varepsilon_S qN_B 2\phi_F)^{1/2}\ ,$$

where V_G is the gate voltage, ε_s is the permittivity of silicon, N_B is the substrate impurity density, W_{poly} is the width of the depletion region in the poly-Si, and $2\phi_F$ is the inversion charge and equals $kT\times\ln(N_B/n_i)$.[1] Since the depletion capacitance $C_{poly}=\varepsilon_s/W_{poly}$, then C_{inv}/C_i is given by

$$(5)\ \frac{C_{inv}}{C_i} = \frac{1}{1+C_i/C_{poly}} = \frac{1}{1+C_i[C_i\left|V_{G'}\right| + (2\varepsilon_S qN_B 2\phi_F)^{1/2}]/\varepsilon_S qN_{poly}}.$$[1]

A plot of C_{inv}/C_i (Fig. 1.3) indicates that when the oxide thickness is 15 Å, $V_G = 1$ V, $N_B = 5\times10^{17}/\text{cm}^3$, and $N_{poly} = 2\times10^{20}/\text{cm}^3$ that C_{inv}/C_i is approximately 0.7. Since $C = \kappa\epsilon_o A/t$, the ratio of C_{inv}/C_i can be related to the ratio of capacitance equivalent oxide thicknesses (t_i/t_{inv}) for a device with poly-depletion. This means that if $t_i = 15$ Å then $t_{inv} = 21$ Å and eliminating the contribution due to poly-silicon depletion can reduce the effective inversion oxide thickness by 6 Å.

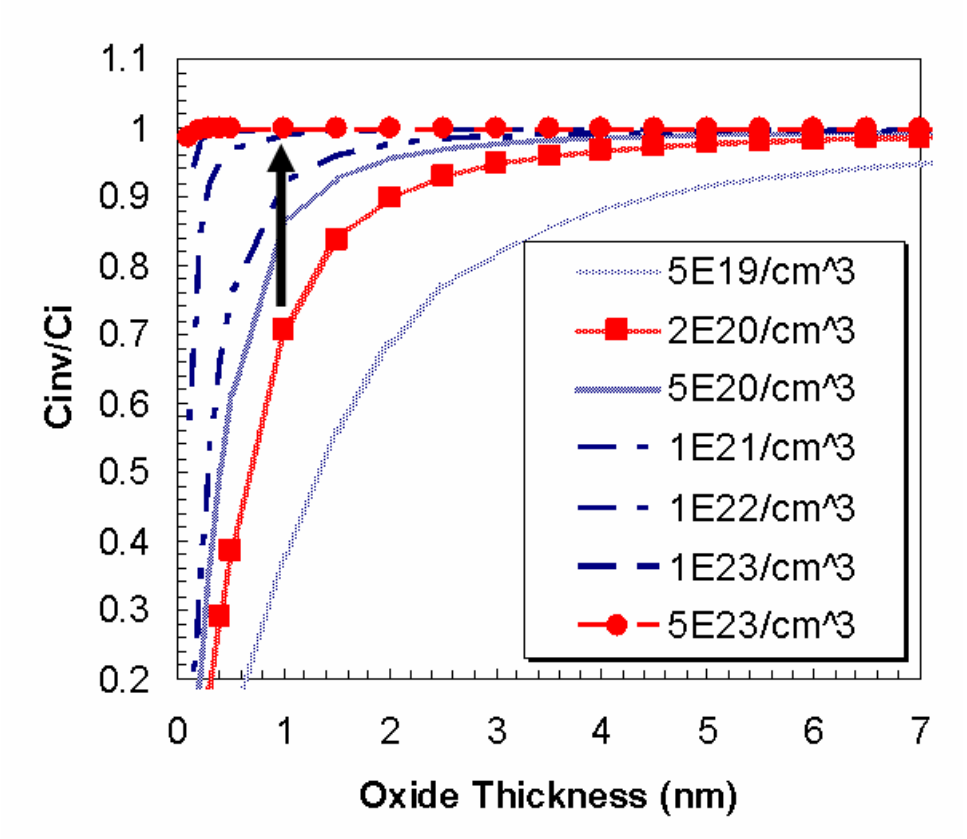

Figure 1.3: A plot of C_{inv}/C_i for different carrier concentrations in the gate electrode. The arrow indicates the boost in inversion capacitance by switching from poly-Si to metal gate electrodes. $V_G = 1$ V, $N_B = 5\times10^{17}/\text{cm}^3$

To overcome the degraded inversion capacitance poly-Si electrodes can be replaced with metal electrodes. Since metals have a shorter Debye length than poly-silicon, meaning a metal has a higher carrier concentration and is more effective at screening charge, no band bending occurs with metal electrodes. This eliminates the depletion capacitance and assists device performance. This can be clearly illustrated if the N_{poly} term in the C_{inv}/C_i equation is replaced with a typical carrier concentration in a metal ($1\times10^{23}/cm^3$). When a metal electrode is employed virtually no gate depletion is observed for scaled oxide thicknesses. This dissertation explores the use of metal gate electrodes on high-κ gate oxides.

Now that the impetus for these recent radical modifications of the MOSFET has been established, each of the following sections will discuss the three specific areas researched in this dissertation. Implementing high permittivity gate dielectrics and metal gate electrodes successfully into a MOSFET structure is a lofty goal, occupying the resources of many industry and university researchers. Progress towards this goal will come by addressing specific aspects of the advanced transistor structure. This dissertation focuses on 1.) the growth conditions required for improving the physical and electrical properties of high-κ gate oxides; 2.) the deposition of metal gate electrodes, their physical and electrical properties, and their thermodynamic stability in contact with high permittivity gate dielectrics; 3.) and the Fermi level pinning of the effective metal gate work function, a phenomena that occurs as a result of creating an interface between the metal gate electrodes and the gate dielectric.

These three independent studies complement and build on the learning obtained in each previous study. Investigating the high permittivity dielectric is a logical starting place since it is the primary reason changes are being made to the gate stack. Next, additional performance gains can be realized by inserting metal gate electrodes. The

metal gate electrodes are used in conjunction with HfO_2 gate dielectrics in this dissertation. Both the physical and electrical properties of metal gate electrodes are explored. Finally, since Fermi level pinning occurs as a result of forming an interface between metal gates and HfO_2 the knowledge obtained in the first two studies has been applied towards further understanding of the possible contributions to the pinning of the metal Fermi level.

1.2 HIGH PERMITTIVITY GATE DIELECTRICS

There are numerous criteria that should be considered when implementing high permittivity gate dielectrics on silicon. Several excellent reviews exist describing what might constitute an ideal gate dielectric candidate.[7,8] However, it is apparent that the "ideal" replacement for SiO_2 may not exist and selection of a gate dielectric will likely be based on a series of compromises. As research in this field has progressed, the seemingly endless list of high permittivity candidates has been slowly whittled away. The industry is currently focused on hafnium based gate dielectrics.

Along with possessing an elevated dielectric constant, a candidate material should have a large band gap and high enough band offsets (~1 eV) with Si to be an effective barrier for both electrons and holes.[9] The high band offsets reduce leakage currents due to tunneling, Schottky emission, and Poole-Frenkel emission, all of which have an exponential dependence on the barrier height ϕ_B.[1] Robertson[9] has calculated band alignments for numerous oxides in contact with silicon. His calculations indicate that ZrO_2, HfO_2, Al_2O_3, Y_2O_3, La_2O_3, Gd_2O_3, and silicates such as $HfSiO_4$ and $ZrSiO_4$ have acceptable band offsets (Fig. 1.4). These results are corroborated experimentally for some of the candidate dielectrics with internal electron photoemission measurements.[10,11,12]

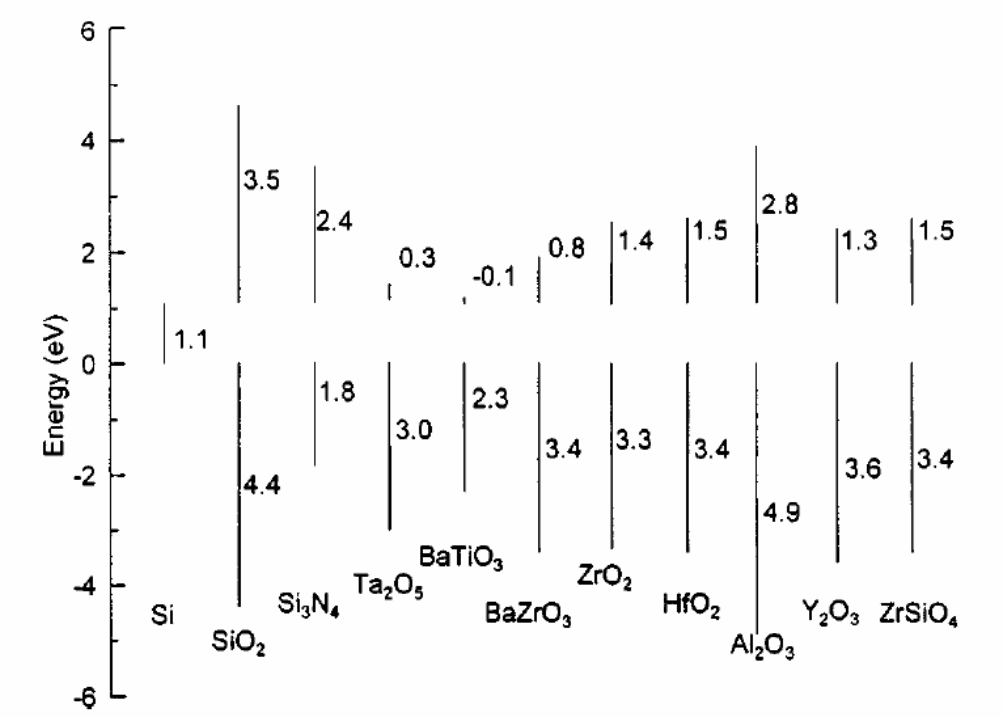

Figure 1.4: Band offsets for high permittivity gate dielectrics in contact with silicon from Robertson[9]

It has also been observed that trade-offs exist between the dielectric constant and the band gap. An empirical trend has been noted where higher permittivity dielectrics have lower band gaps (Fig. 1.5).[13] Because of this relationship, ZrO_2 and HfO_2 with a κ ~ 20 and E_g ~ 5.8eV appear to be promising candidates.

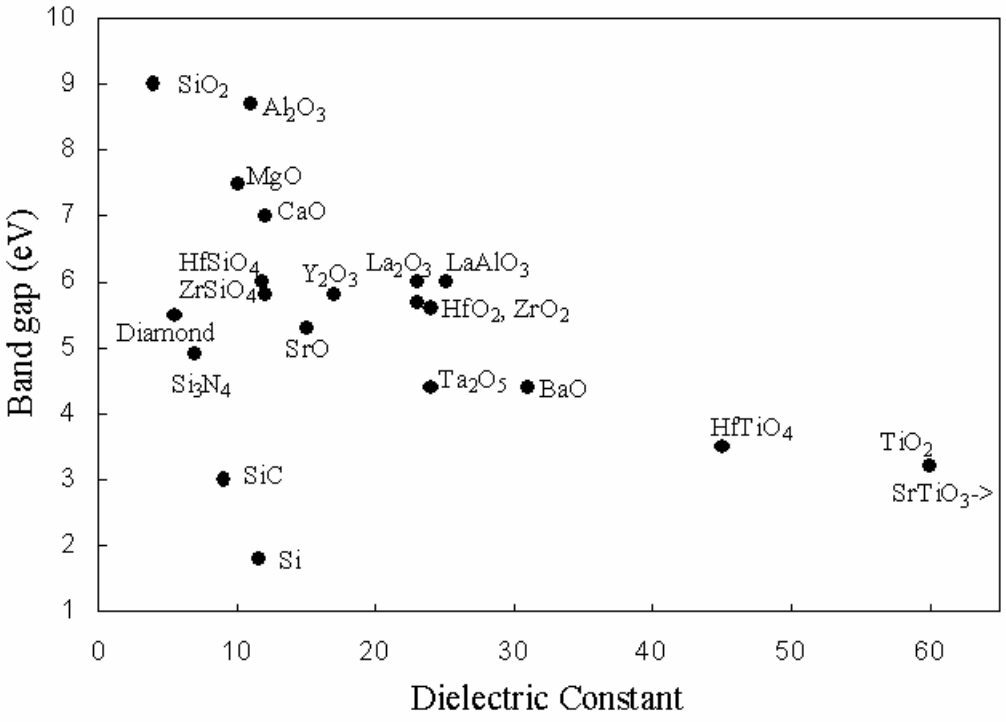

Figure 1.5: Plot of dielectric constant versus band gap.[14]

Another factor for selection of a high permittivity gate dielectric is its thermodynamic stability when in contact with silicon. In typical integrated circuit manufacturing subsequent thermal processing requires the dielectric-silicon interface to withstand temperatures of approximately 1000 °C. This problem was first considered by Hubbard and Schlom who examined thermodynamic data for binary oxides in contact with silicon.[15] In their study, binary oxides were eliminated as gate dielectric candidates if their reaction with silicon resulted in the reduction of the metal oxide to a pure metal (Eq. 7), the reduction of a metal oxide to a metal silicide (Eq. 8), the reduction of a metal oxide to a less oxygen-rich metal oxide and SiO_2 (Eq. 9), or the conversion of a metal oxide to a more oxygen rich metal oxide and a metal silicide (Eq. 10). The reactions that were tested for a negative Gibbs free energy are

$$(7)\ \mathrm{Si} + \mathrm{MO_x} \rightarrow \mathrm{M} + \mathrm{SiO_2}$$
$$(8)\ \mathrm{Si} + \mathrm{MO_x} \rightarrow \mathrm{MSi_z} + \mathrm{SiO_2}$$
$$(9)\ \mathrm{Si} + \mathrm{MO_x} \rightarrow \mathrm{MO_w} + \mathrm{SiO_2}$$
$$(10)\ \mathrm{Si} + \mathrm{MO_w} \rightarrow \mathrm{MO_x} + \mathrm{MSi_z}$$

where MO_x is more oxygen rich than MO_w.

In addition, metal oxides in contact with silicon that have a negative Gibbs free energy towards the formation of a ternary metal silicate phase with a co-reaction product of MSi_x (Eq. 11), M (Eq. 12), or SiO_2 (Eq. 13) were also considered to be thermodynamically unstable in contact with silicon. The following three equations give the reactions that were considered.

$$(11)\ \mathrm{Si} + \mathrm{MO_x} \rightarrow \mathrm{MSi_z} + \mathrm{MSi_xO_y}$$
$$(12)\ \mathrm{Si} + \mathrm{MO_x} \rightarrow \mathrm{M} + \mathrm{MSi_xO_y}$$
$$(13)\ \mathrm{Si} + \mathrm{MO_x} \rightarrow \mathrm{SiO_2} + \mathrm{MSi_xO_y}$$

Li_2O, BeO, MgO, CaO, SrO, Sc_2O_3, Y_2O_3, RE_2O_3 (RE= rare earth), ThO_2, UO_2, ZrO_2, HfO_2, and Al_2O_3 were predicted to have thermodynamic stability in contact with silicon at 1273 K. These calculations for solid-phase reactions provide a starting place for selection of potential gate dielectrics. Of the aforementioned materials Y_2O_3, La_2O_3, ZrO_2, HfO_2, Al_2O_3, and some of their ternary oxides have garnered the most intensive investigations.

Although the above calculations predict stability, further experimentation on the Y_2O_3, La_2O_3, ZrO_2, HfO_2, and Al_2O_3 systems has uncovered some thermodynamic instability that might be problematic for device manufacturing. When ZrO_2 and HfO_2 are deposited on Si with a pre-grown SiO_2 interfacial layer a window of optimum oxygen partial pressures for annealing has been observed. At low oxygen partial pressures, the SiO_2 interfacial layer can be decomposed ultimately resulting in zirconium silicide formation with the substrate. This is believed to occur at temperatures and pressures where the reaction

$$(14)\ 2Si(s) + O_2(g) \rightarrow SiO(g)$$

is favorable.[16,17,18,19] Stemmer, et al., report that at 1000 °C and $p_{O2} < 1\times10^{-7}$ Torr the formation of SiO(g) is favorable and the presence of zirconium silicide is detected with transmission electron microscopy (TEM). Alternatively, if the oxygen partial pressure is increased so that $p_{O2} > 1\times10^{-4}$ Torr excess oxygen readily diffuses through the ZrO_2 to react with the substrate. This increases the SiO_2 interfacial layer thickness. Selecting an oxygen partial pressure between these two annealing conditions is required to balance the

growth and decomposition of the interfacial layer. A similar annealing window is expected for HfO_2 gate dielectrics.

It has also been shown that the SiO_2 interfacial layer can decompose at temperatures significantly lower than those required for the evolution of SiO(g). This can even occur during the HfO_2 growth process itself. This is surprising considering HfO_2 growth typically proceeds with a >1000× higher oxygen flux than Hf flux. Because of this Copel and Reuter propose an alternative model for the SiO_2 decomposition in this scenario.[20] This model proposes that if HfO_2 is deposited with a pre-existing concentration of oxygen vacancies (V_o) an exchange between V_o from the HfO_2 for oxygen from SiO_2 interfacial layer can occur. This results from the strong affinity for oxygen and the high oxygen diffusivity in HfO_2. This process reduces the interfacial layer via the reaction

$$(15)\ SiO_2(s) + 2V_O \rightarrow Si(s)\ .$$

It has been speculated that the silicon excess will need to be oxidized or diffused away from the substrate for acceptable electrical characteristics.

Even when operating in the window of optimum oxygen partial pressures, ZrO_2 and La_2O_3 are observed to behave differently in contact with the SiO_2 interfacial layer. One striking difference between the two systems is that upon annealing ZrO_2-SiO_2 tend to phase separate[16,17] while La_2O_3-SiO_2[18,21,22,23] reacts to form a silicate even though both systems have stable silicate compositions that extend to low temperatures on the pseudo-binary phase diagrams. The explanation for this apparent discrepancy lies in the fact that the La_2O_3:SiO_2 system has silicate phases that melt congruently compared to the ZrO_2:SiO_2 system where the silicate phase forms via a peritectic reaction (Fig. 1.6). The

peritectic reaction requires solid-state diffusion of Si and Zr through highly refractory solids. This is a kinetic limitation to $ZrSiO_4$ formation. Due to this kinetic limitation a metastable miscibility gap exists which drives the ZrO_2:SiO_2 system to phase separation. The Y_2O_3:SiO_2[24,25,26] and HfO_2:SiO_2[27] systems behave similarly to the La_2O_3:SiO_2 and ZrO_2:SiO_2 systems, respectively. The tendency towards phase separation is also observed when the as deposited dielectric is a zirconium or hafnium silicate.

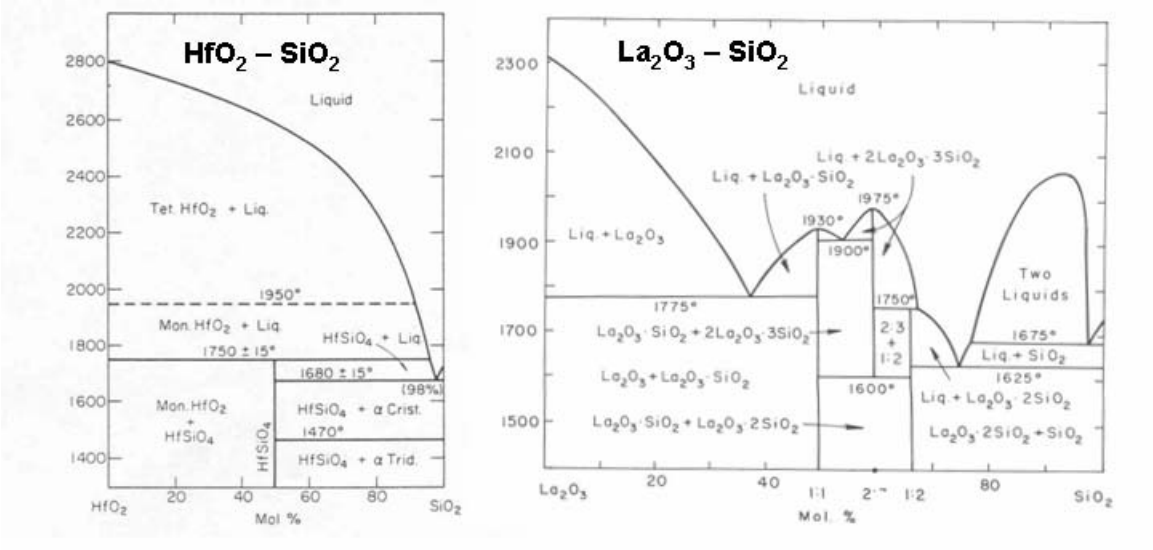

Figure 1.6: Phase diagrams for $HfO_2 – SiO_2$ and $La_2O_3 –SiO_2$.[28]

Even though ZrO_2 and HfO_2 can be engineered to possess interface stability with the substrate, incompatibilities exist between ZrO_2[29,30] and HfO_2[31] and the gate electrode when it is deposited using low pressure chemical vapor deposition (LPCVD) from silane (SiH_4) precursor. Large inhomogeneous grains extending up from the HfO_2 gate dielectric are observed with dark field optical microscopy and transmission electron microscopy (TEM). High leakage current is also typical when poly-Si growth temperatures of 620 °C are used. An Al_2O_3 capping layer over the HfO_2 eliminates the presence of large grains and improves the leakage current by nearly 8 orders of magnitude. The inhomogeneous grains are thought to be due to metal induced crystallization where locations on the HfO_2 surface might be reduced by the CVD ambient. Since bulk thermodynamic calculations do not support this conjecture, it is thought that the reactions may only occur at grain boundaries where bonding is more disrupted. This would also explain the distribution of inhomogeneous grain growth.

One disadvantage of many high-κ gate dielectrics is that they possess a polycrystalline microstructure. This is thought to be undesirable because polycrystalline dielectrics possess grain boundaries which are known to be high diffusivity pathways in ceramics[32] and may potentially behave as a conduit for elevated electrical leakage. Grain boundary diffusion is of particular concern with doped poly-Si electrodes where the penetration of dopant atoms into the substrate can cause undesired threshold voltage shifts. Modeling studies indicate that B and O can penetrate the depth of a typical HfO_2 dielectric thickness at 900 °C via a grain boundary diffusion mechanism.[33] To circumvent this problem amorphous hafnium and zirconium silicates have been investigated. Silicates with low concentrations of the Zr and Hf cation (~2-8%) are shown to retain their amorphous structure and demonstrate interface stability with silicon to temperatures of 1050 °C.[34,35,36] Another study that evaluated a range of Zr-Si-O

compositions by co-sputtering from a Zr and Si targets indicates that Zr concentrations between 6 at.% - 15 at.% produce an effective dielectric constant of 7.5-12.4.[37] Additionally, when chemical solution deposited films were investigated over the entire composition range $(ZrO_2)_x$:$(SiO_2)_{(1-x)}$ the intermediate silicate compositions were shown to exhibit dielectric constants that are less than the weighted average of the terminal compositions ($\kappa = 4$ for SiO_2 and $\kappa = 22$ for ZrO_2). [38]

It is the addition of glassy SiO_2 that suppresses the onset of crystallization in silicates compared to the binary Zr and Hf oxides. The onset of crystallization is composition dependent and occurs via phase separation of ZrO_2 and SiO_2 resulting in crystallites of ZrO_2 embedded in a SiO_2 matrix.[38,39] For alloys of ≥ 50% ZrO_2, phase separation generally occurs at T ≤ 800 °C, and for alloys of ≤ 25% ZrO_2, phase separation is not detected until T ~1000 °C. Another study has attributed the phase separation process to spinodal decomposition for HfO_2 deficient films (40% HfO_2) characterized by a constant wavelength for phase distribution, and to nucleation and growth for HfO_2 rich films (80% HfO_2) which exhibit a more random arrangement of phases.

Hafnium silicate dielectrics with a ~0.52 Si/Zr ratio are shown to resist boron penetration up to 950°C.[40] It is believed that after the phase separation and crystallization occurs, grain boundary diffusion is responsible for the onset of enhanced B diffusivity compared to pure SiO_2 dielectrics. A similar study indicates that Hf silicate films resist P and As diffusion up to temperatures of 1000 °C and 1050 °C, respectively.[41] The alloying of hafnia (HfO_2) with alumina (Al_2O_3) has also proven to be successful at suppressing crystallization of Hf-based gate dielectrics.[42]

Another demonstration of suppressed crystallization, reduced dopant penetration, and improved electrical properties has been obtained by the nitridation of Hf and Zr-based gate dielectrics. Nitrided films have been obtained by a variety of techniques

including post-deposition annealing in NH_3,[43] pre-deposition annealing in NH_3,[44] reactive sputtering,[45] oxidation of sputtered HfN layers,[46,47] oxidation and nitridation via post-deposition annealing of HfSi in NH_3 (the source and partial pressure of oxygen is not specified),[48] and MOCVD in the presence of N_2 and NH_3 (the source and partial pressure of oxygen is not specified).[49] Calculations indicate that the addition of nitrogen reduces the band gap of HfO_2 by ~1.2eV.[50] This is because the presence of N introduces gap states above the valence band edge of HfO_2. The same article also indicates that it is unclear why N stabilizes the amorphous phase, but speculates that one reason might be due to the fact that N lowers the mean coordination of HfO_2, a characteristic of glass forming materials.[51,52]

Compared to SiO_2, the introduction of high permittivity dielectrics present a variety of factors that might contribute to degraded device mobility and reliability. These include a higher density of defects at the Si interface due to bonding constraints,[51,52] increased Si roughness, fixed charge in the dielectric, channel doping impurities, and remote phonon scattering.[53] To improve mobility the growth of a high quality SiO_2 interfacial layer is considered desirable between the Si and the high-κ dielectric. The interfacial layer reduces the number of interface trap states and places fixed charges in the high-κ dielectric further from the interface. The presence of a low-κ SiO_2-based interfacial layer obviously degrades the capacitance of the oxide stack. Therefore, selecting the interfacial layer thickness is a trade-off between mobility and capacitance. Even with an interfacial layer, high permittivity dielectrics are observed to possess a higher density of interface traps than a pure SiO_2 dielectric. Approaches to remedy this problem include high temperature forming gas anneals,[54,55] deuterium anneals,[56] and ALD growth using $HfCl_4$ and D_2O (opposed to H_2O).[57]

Charge trapping under voltage stressing is responsible for unacceptable threshold voltage shifts under accelerated reliability testing.[58] Because of this, an increased focus has been placed on identifying specific defects responsible for the electron traps. Recent electron spin resonance studies have identified point defects at the Si/high-κ dielectric interface[59] and within the HfO_2 bulk.[60] It has also been recently shown that inelastic electron tunneling spectroscopy (IETS) can be used as an effective tool for identifying traps in high-κ dielectrics.[61] Other studies of specific defects include calculations which indicate that hydrogen acts as a shallow donor in many of the candidate high-κ gate oxides[62] and a recent paper that includes a model for the presence of excess oxygen which provides electronic states at the high-κ - SiO_2 interface.[63] Ambient exposure of the high-κ gate dielectric prior to electrode deposition can also introduce undesired defects. There have been recent studies on the role of ambient H_2O and carbon-species on the formation of hydroxide, carbonate, and alkoxylate species.[64,65,66]

This section has reviewed advances on implementing high-κ gate dielectrics in silicon based MOSFETs. The field has progressed from identifying appropriate materials properties and evaluating candidate materials to the current research state which is to identify specific defects and to enhance device properties. This section provides background information for the experiments discussed in Chapter 3 which discusses how film growth conditions influence the material and electrical properties of HfO_2. Further work remains before high-κ gate dielectrics are successfully implemented in integrated circuit manufacturing.

1.3 METAL GATE ELECTRODES

To meet the scaling trends and overcome degraded inversion capacitance due to poly-depletion, metal gate electrodes are being evaluated as a replacement to poly-silicon electrodes.[67] Metal gate electrodes have the added benefit of reducing the gate resistance and eliminating the threat of boron penetration from p+ poly-silicon into the channel region.

For bulk CMOS devices, simulations indicate that the desired work function for NMOS (PMOS) electrodes is near the conduction (valence) band edge of silicon.[68,69] These simulation studies imposed the constraint of a constant off current (I_{off}) for a sub-nominal length device. This constraint means that if the metal work function is shifted towards the middle of the Si band gap, the substrate doping has to be reduced to maintain a constant I_{off}. However, reducing the substrate doping severely degrades the short channel performance of a MOSFET, as evidenced by exacerbated V_t roll-off (Fig. 1.7) at short channel lengths. Reducing the substrate doping lowers the potential barrier and increases the depletion width between the source and the channel regions. Therefore, as the gate length is reduced electric fields from the drain contribute to lowering this potential barrier. Because of the reduced barrier height current can flow across the channel, and the device is partly on even with little or no gate voltage applied. This phenomenon is referred to as drain induced barrier lowering (DIBL) (Fig. 1.8). DIBL manifests itself as a degraded subthreshold swing, a measure of how rapidly the drain current responds to the gate bias. The increased V_t caused by shifting the work function towards the middle of the silicon gap results in a lower inversion charge density for the same gate voltage which degrades the current drive of the MOSFET in saturation ($I_{d,sat}$). Ultimately, these simulations conclude that work functions of ~4.1 eV (~5.2 eV) near the conduction (valence) band edge are required to optimize NMOS (PMOS) device

performance for bulk silicon substrates. This requisite severely limits the number of materials that can be used as metal gate electrodes. However, an alternative solution exists. Fully-depleted silicon-on-insulator (FDSOI) devices with an appropriate silicon thickness can be produced to reduce the impact of short channel effects. Because of this, the channel regions in FDSOI devices can be made with low silicon doping to improve mobility and metal electrodes with work functions closer to mid-gap are acceptable.[70]

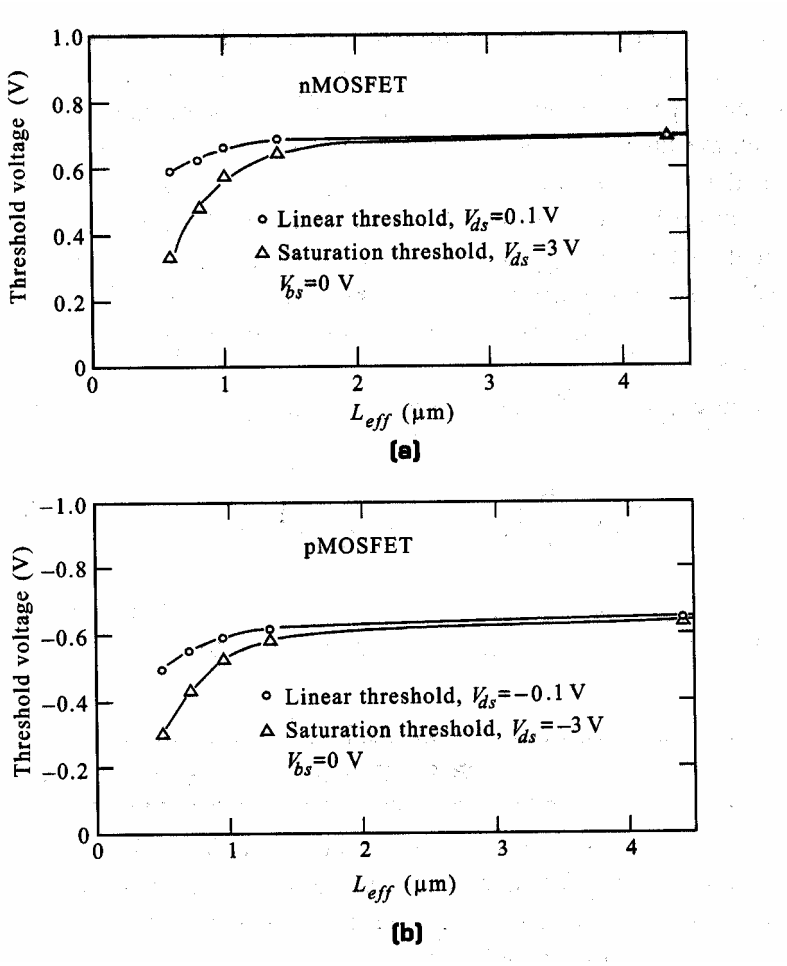

Figure 1.7: Example of threshold voltage roll-off at short channel lengths.

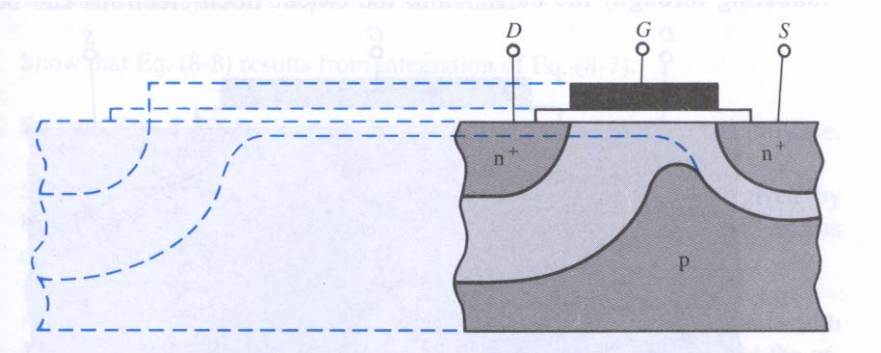

Figure 1.8: Schematic showing the overlap of the source and drain depletion regions in short and long channel MOSFETs which results in drain induced barrier lowering (DIBL).[71]

A quick review of the work functions of the elements[72] shows a periodicity between work function and atomic number. Work functions increase from left to right across a row on the periodic table (Fig. 1.9). This indicates that metals with work functions above the conduction band edge of Si (<4.1 eV) are typically in the first three columns of the periodic table. Alternatively, metals with work functions below the valence band edge of Si (>5.2 eV) tend to be late transition metals. In particular, the platinum group metals such as Pt, Ir, Os, Au, Ni, Ru, Pd, and Rh have high work functions. The vast majority of the transition metals have work functions that exist within the band edges of silicon (4.1 eV < ϕ_m < 5.2 eV). The work functions of metals have been studied using a variety of techniques. These include the photoelectric effect, thermionic emission, field emission, contact potential difference, and extracted from MOS capacitors. These techniques do not necessarily produce the same value which complicates the search for candidate materials. In this dissertation the effective work function is extracted using MOS capacitors. This is discussed further in Chapter 4 and Chapter 5.

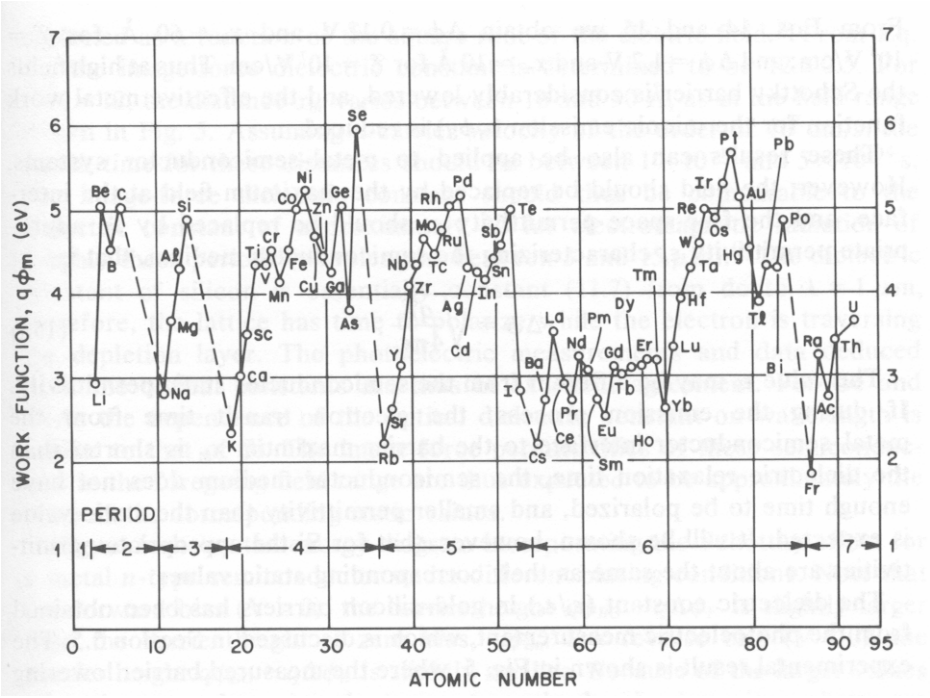

Figure 1.9: Plot of work function versus atomic number. Work functions are generally observed to increasing moving across a row of transition metal elements.

To further narrow the list of viable metal gate electrodes, candidates must also possess thermal stability up to the dopant activation temperatures of approximately 900-1000 °C. Thermal stability includes the absence of gross reactions between the dielectric and other surrounding materials, no inter-diffusions with surrounding materials, sufficient bulk phase stability, and smooth interfaces with the dielectric. Due to these stringent thermal requirements refractory metals such as W, Re, Ta, and Mo have attracted interest.

Metal nitrides and carbides have also gathered attention as metal gate electrodes. These materials are renowned for their use as diffusion barriers in the semiconductor industry. Transition metal nitrides and carbides are comprised of a face-centered-cubic metal structure with nitrogen or carbon atoms occupying the octahedral interstices. This results in the rock-salt structure (NaCl). Since N and C occupy interstices the lattice parameter is typically only ~5% larger than that of the pure metal compound. Stuffing the interstices with N or C helps give these materials their excellent diffusion barrier properties. These materials exhibit metal-like conduction, but at the same time are highly refractory compared to the pure metal constituent. It is believed that a mixture of metallic, covalent, and ionic bonding character is responsible for this behavior.[73] There have been numerous studies on the work function of interstitial nitrides for electrode and emitter applications. This includes MoN,[74] WN,[75] NbN,[76] TaN,[75,77] TiN,[75,78,79,80] ZrN,[76] and HfN[81] among others. TiAlN has also been widely studied as a metal gate electrode.[82] Although it is a ternary metal nitride, it is more closely related to the binary nitrides than the amorphous ternary metals because this compound exists in the rock salt structure for Al:Ti ratios <0.40 and in a mixture of rock salt and wurtzite structures for >0.40 Al:Ti ratio.[83] TiAlN loses its conductive properties with increasing presence of the AlN wutzite phase.

Ternary alloys of a transition metal (TM), silicon, and nitrogen have also been widely investigated for their properties as diffusion barriers. These films are found to exist in a highly metastable amorphous structure.[84] This property makes them excellent diffusion barriers to elevated temperatures. Ta-Si-N is currently being investigated as a stable NMOS electrode candidate.[75,85,86,87]

Another problem is the need to integrate two metals with different work functions to build both NMOS and PMOS devices. This is easily done with poly-silicon electrodes by ion implanting n-type or p-type dopants into NMOS or PMOS electrodes, respectively. The implantation is performed selectively by patterning the NMOS region with photoresist while implanting dopants into the PMOS regions and vice-versa. The implants shift the Fermi energy of n-type poly-silicon towards the conduction band and shift the Fermi energy of p-type poly-silicon towards the valence band to achieve the appropriate work functions and low device V_ts.

Different integration approaches have been proposed for metal gates. Both conventional integrations and replacement gate[88,89] integrations have been proposed. Replacement gate integrations dramatically reduce the temperatures that the metal gate must withstand because the source/drain activation anneals are performed before the metal gate is deposited. The other integration approaches can be classified into one of four types. These include stacked dual metal gate integration, metal alloy integration, nitrogen modulation integration, and fully-silicided metal gate (FUSI) integration.

The integration approach that most easily accommodates vastly different metals for NMOS and PMOS electrodes is the stacked dual metal gate integration (Fig. 1.10). This integration involves depositing one metal over both the NMOS and the PMOS regions. Then patterning one of the two regions and removing the electrode using a wet etch chemistry that is selective to the underlying gate dielectric. A second metal can then

deposited over the first metal. The most difficult aspect of this integration is the plasma etching two different gate stacks of different heights. This integration has been demonstrated on Si_3N_4 gate dielectric[90] and on HfO_2 gate dielectrics.[91]

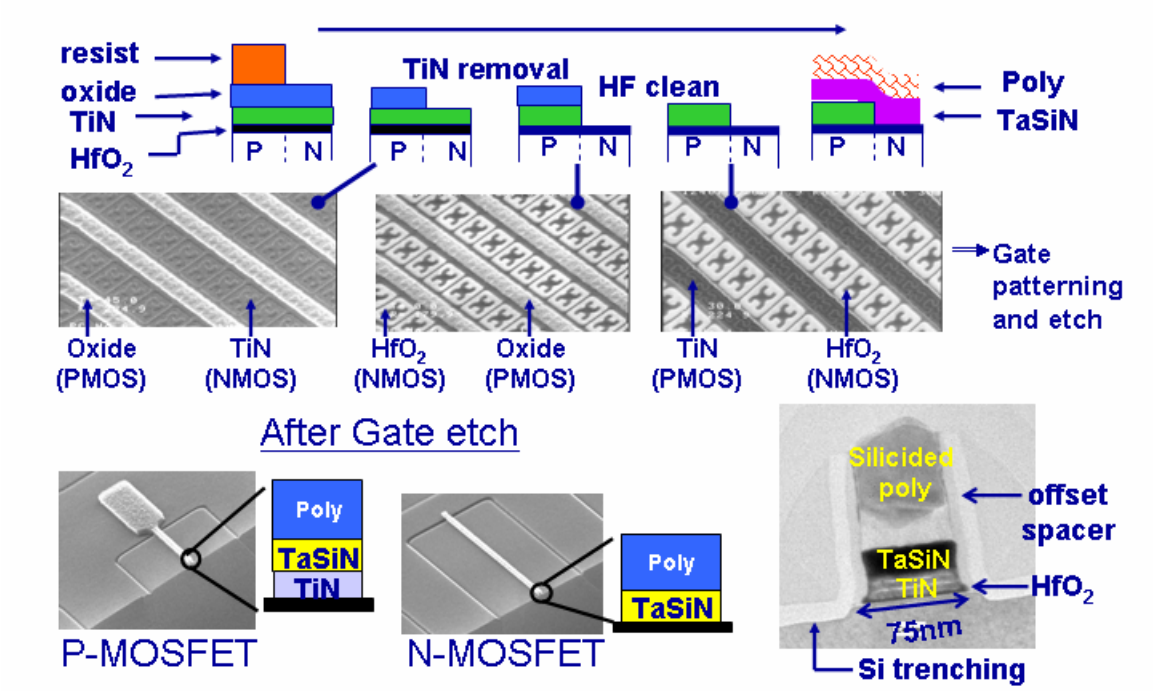

Figure 1.10: Process flow for the stacked dual metal gate integration. The difficulty in this approach is that two gate stacks of different heights need to be etched simultaneously.

In the metal alloy approach two metals are initially deposited on top of each other. Either the NMOS or PMOS region is then patterned so that the top metal can be selectively removed. A high temperature annealing process is then used to inter-diffuse the two metals. This leaves an inter-diffused metal for one of the electrodes and an elemental metal for the other electrode (Fig. 1.11). This approach has been performed using Ru-Ta[92,93], Ti-Ni[94], and Pt-Ta[95] alloys. The alloyed electrode approach has two foreseeable problems. First, it may be difficult to get one alloy system to span the entire 1.1 eV range to meet the NMOS and PMOS work function requirements. Second, some of the elements used in the alloy may not be thermally stable in contact with a high permittivity dielectric. This will be discussed further in Chapter 4.

The nitrogen modulation integration has been reported in two forms (Fig. 1.12). The first method is to ion implant nitrogen into a metal to shift its work function. This has been demonstrated for Mo-based electrodes,[96,97] and for TiN-based electrodes where the N concentration is modulated via implantation of N.[98] Adjusting the nitrogen concentration has also been accomplished by solid-state diffusion of nitrogen from a nitrogen-rich film into a nitrogen-deficient film.[99] Like the alloy approach, it may be difficult to span the entire work function range to meet the NMOS and PMOS electrode requirements by implanting nitrogen.

The fully-silicided integration has also shown some promise toward work function modulation.[100] In this approach the gate silicide process, which is normally used as a contact to the poly-Si electrodes, is performed in a way that the metal contact consumes all the poly-Si forming a metallic silicide all the way down to the gate dielectric interface (Fig. 1.13). Work function modulation is achieved by controlling the dopants in the poly-Si. Although there is still debate about the exact mechanism, it is believed that the silicide reaction snow plows the dopants in the poly-Si down to the

dielectric interface. Like some of the other approaches this technique is limited in the magnitude of work function modulation that can be achieved. Also, there is concern that the silicide reaction might “spike” through defects into the oxide forming defects in the substrate.

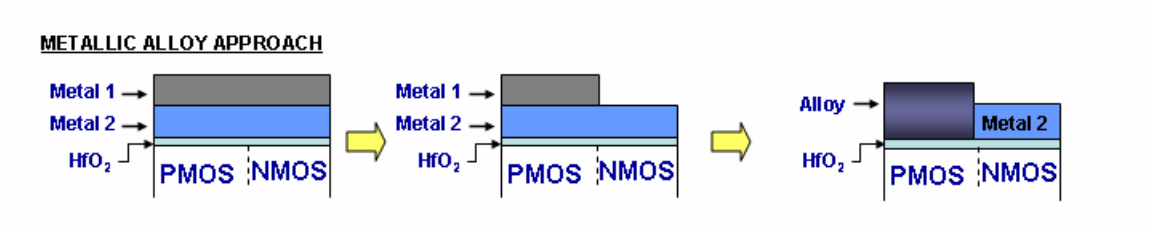

Figure 1.11: Process flow for the metallic integration showing how two metals are formed by depositing a metal stack, selectively patterning and etching the top metal, and annealing to alloy the bi-metal stack.

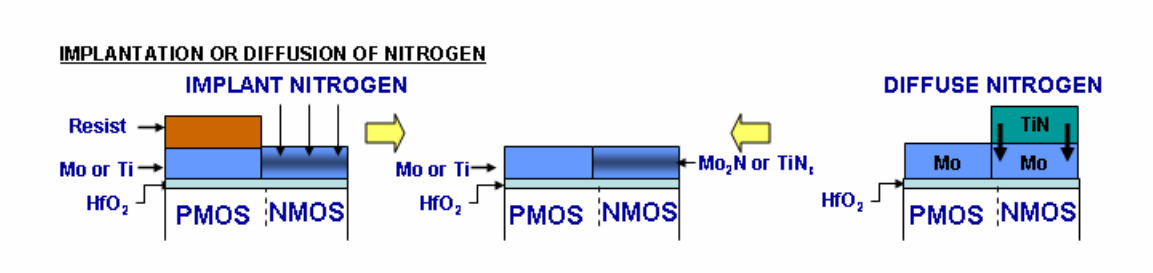

Figure 1.12: Process flow for the ion implantation and solid-state diffusion of nitrogen to form a nitrogen-rich (NMOS) and a nitrogen-deficient electrode (PMOS)

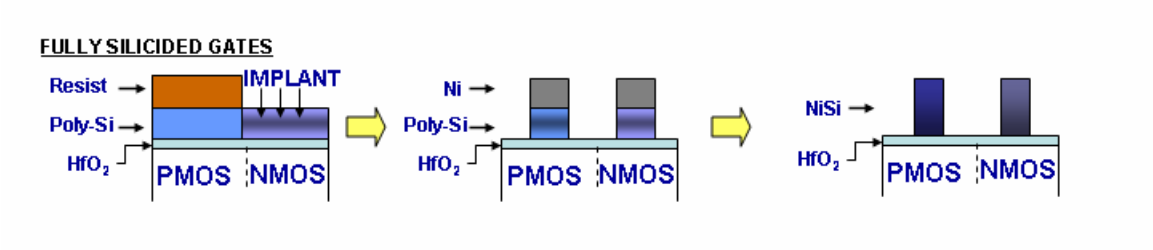

Figure 1.13: Process flow illustrating the ion implantation of different dopants into the poly-Si followed by NiSi gate electrode formation

Chapter 4 will discuss candidate metal gate electrodes, common stability issues encountered during high temperature annealing, and discuss which materials hold promise for implementation into future CMOS integrations.

1.4 FERMI LEVEL PINNING

A roadblock to successful implementation of metal gate electrodes with the proper work functions is Fermi level pinning. Fermi pinning is a consequence of forming an interface between a metal and a dielectric (or semiconductor). When an interface is formed, the effective metal work function becomes "pinned" at a different energy than its vacuum work function. This results from interfacial charge exchange between the metal Fermi level and gap states at the metal-dielectric interface causing it to shift with respect to its unpinned location. A recent comprehensive review of Schottky barrier concepts has been published.[101]

Fermi level pinning of poly-Si[102] and metal electrodes[103,104] on HfO_2 has been investigated, and Fermi pinning models have been extensively tested on a broad class of interfaces.[105,106,107,108] The most widely accepted of these models is the metal induced gap states (MIGS) model. The origin of the gap states in the MIGS model is from the dangling bonds of under-coordinated surface atoms. These dangling bonds produce surface states that are dispersed in continuum at energies throughout the band gap of the dielectric. The wave function for surface states is given by $\psi = u(r)exp(ik_{\parallel}r)exp(-ik_{\perp}z)$.[109] The two components of this equation are related to electron propagation in the plane of the surface and electron propagation normal to the surface. For electrons traveling parallel to the surface the wave vector $k_{\parallel}$ is real, and $\psi = u(r)exp(ik_{\parallel}r)$.

However, for electron propagation normal to the surface $k_\perp$ is complex. This is because the $E\text{-}V(z)$ term under the square root in the expression $k_\perp = (2m[E\text{-}V(z)]/\hbar^2)^{1/2}$ is negative. This term is negative due to the potential $V(z)$ being greater than the electron energy when an electron tunnels outside the crystal or when an electron tunnels into the crystal bulk. Therefore, the $exp(-ik_\perp z)$ term results in an exponential decay of the electron wave function for directions normal to the surface. These are often referred to as evanescent states. Similar to a surface state on a dielectric, a cleaved metal surface also has a surface wave function that decays exponentially into vacuum. In the MIGS model, when a metal is placed in contact with a dielectric, the metal surface states induce the gap states in the dielectric. This results in interfacial charge exchange between the metal and the dielectric gap states causing the metal Fermi level to shift with respect to its unpinned location towards a characteristic energy level in the semiconductor. In the MIGS model this characteristic energy is referred to as the charge neutrality level ($\phi_{CNL,d}$). The charge neutrality level is the location of the highest occupied surface state in the dielectric band gap. The charge neutrality level has been described as the position where the surface states change from acceptor-like to donor-like character. Therefore, when the two surfaces are brought into contact, charge is exchanged between the metal and the dielectric surface states resulting in the formation of an interfacial dipole. The magnitude of the interfacial dipole depends on the pinning strength of the semiconductor which is defined by the value of the Schottky pinning parameter (S). The barrier height between a metal Fermi level and the dielectric conduction band depends on the pinning parameter and is given by $\Phi_b = S(\phi_{m,vac} - \Phi_{CNL,d}) + (\Phi_{CNL,d} - \chi_d)$.[9,110] In the Schottky, or weak pinning, limit $S=1$, while in the Bardeen, or strong pinning, limit $S=0$ (Fig. 1.14). The magnitude of Fermi pinning in a MOS capacitor can also be measured in terms of an effective metal work function ($\phi_{m,eff}$), as opposed to barrier height shifts. The effective

work function is related to the vacuum work function $(\phi_{m,vac})$ by $\phi_{m,eff} = \phi_{CNL,d} + S(\phi_{m,vac} - \phi_{CNL,d})$.[103] It should be noted that the gap states in the MIGS model are intrinsic to any metal-dielectric interface.

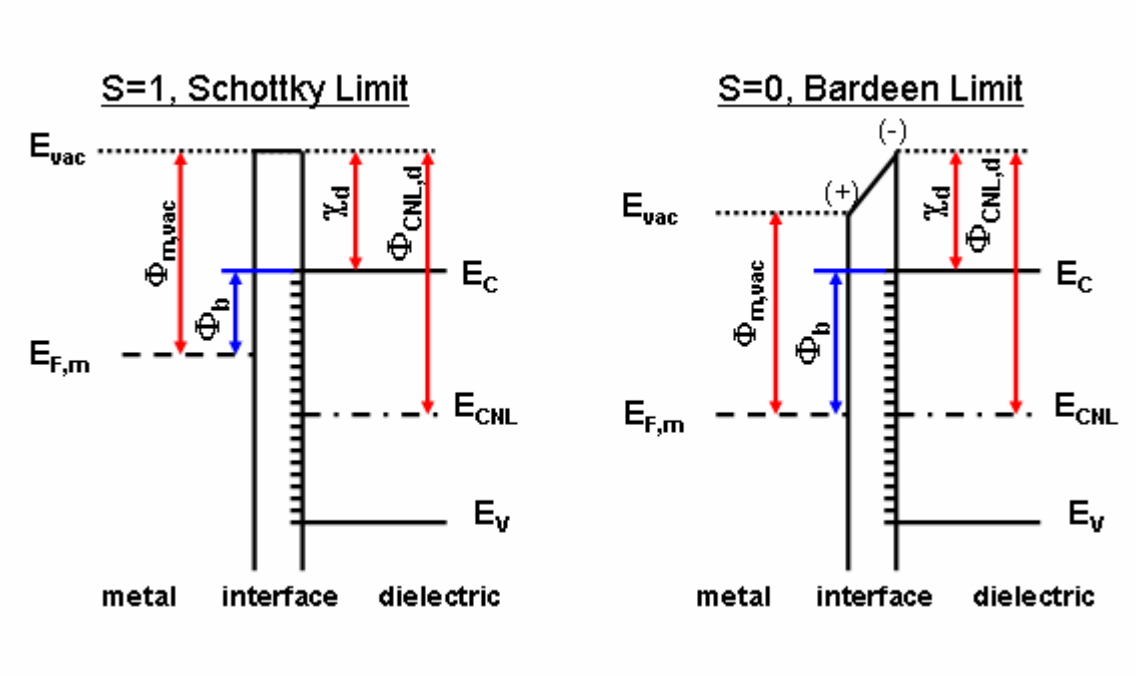

Figure 1.14: Schematic of Fermi pinning in the Schottky or weak-pinning limit and in the Bardeen or strong-pinning limit.

In the linear approximation the pinning strength is given by

$$S = \frac{1}{1 + (e^2 N\delta)/\varepsilon\varepsilon_o}$$

where N is the density of interface states per unit area, δ is the penetration depth of the interface states, e is the electronic charge, $\varepsilon\varepsilon_o$ is the dielectric constant times the permittivity of free space.[111] Tersoff later proposed that S is proportional of the inverse of the electronic portion of the dielectric constant ε_∞[112] while Monch[113] empirically determined that the pinning strength is related to the electronic contribution to the dielectric constant by the following relation

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}.$$

A plot of *1/S-1* versus *1-*ϵ_∞ reveals a dependence on the pinning parameter and the electronic contribution to the dielectric constant (Fig. 1.15). The plot indicates that highly ionic materials with large band gaps tend to have low pinning strength, while smaller band gap materials are inclined to be stronger pinning materials. This is due to the fact that wide gap materials present a larger tunneling barrier, thus reducing the penetration of the metal wave function into the dielectric (δ), and because wide gap materials have a lower density of interface states N at the center of their band gap.

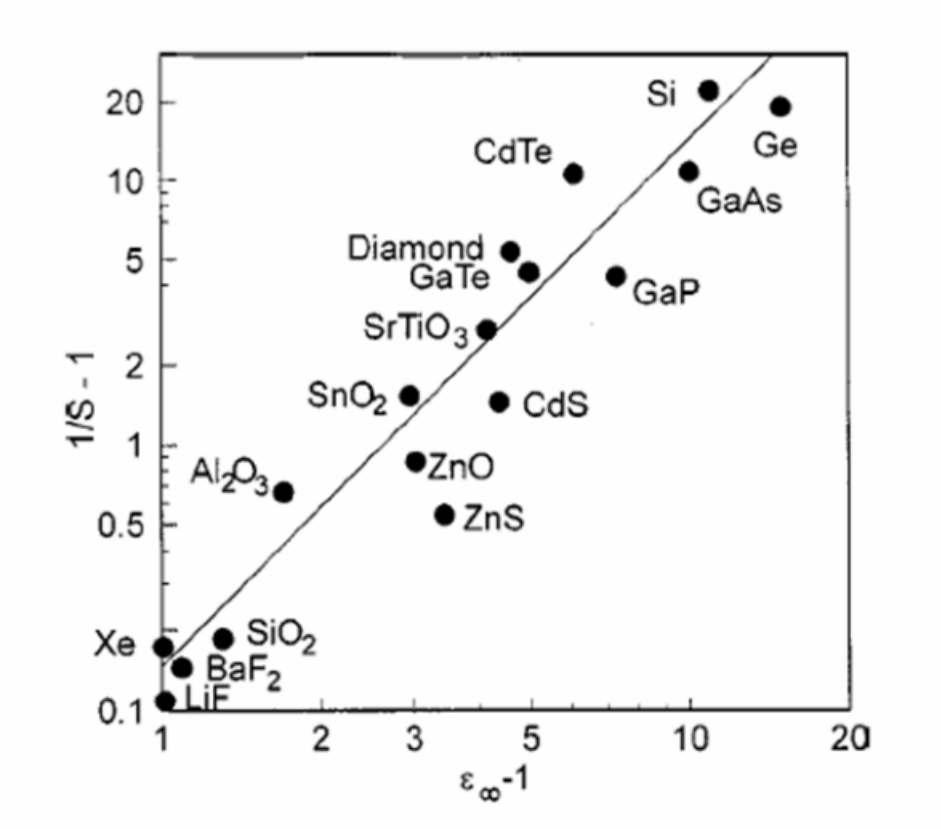

Figure 1.15: Plot showing empirical relationship between pinning parameter (*S*) and electronic component of the dielectric constant, ε_∞.

Other models have been proposed where the states responsible for Fermi level pinning have an extrinsic origin. These include the unified defect theory where a specific defect, with a high density of states at a given energy is responsible for the pinning behavior; disorder-induced gap states, where variations in bond length and bond angle at an interface result in states dispersed across the band gap; and finally the effective work function theory where the effective work function is determined by the work function of a metallic species that precipitates at the interface. In this work these models will be considered to the extent that extrinsic defects might account for disagreement between experiment and the MIGS model.

Furthermore, there has been some effort at modifying the extent of Fermi level pinning by dosing surface with intra-layers that can modify the interface dipole. One such paper reports that hydrogen and cesium intra-layers between SiO_2-Si interfaces can produce large changes in the band alignment.[114] The Fermi level pinning experiment presented in this work observes similar shifts in band alignment depending on whether the interface is hydrogen or oxygen-rich.[115] An explanation of the results based on oxygen vacancy defects and interface dipoles is presented.

This section has reviewed the origin of Fermi level pinning in the MIGS model and how it is responsible for causing undesired shifts to the metal work function. This dissertation investigates the sources of Fermi level pinning with HfO_2 based gate dielectrics in Chapter 5. The intrinsic component of Fermi pinning may pose formidable challenges to the implementation of metal gate electrodes with the proper threshold voltages.

1.5 SCOPE OF THIS WORK

The vast majority of the experimental work for this dissertation was performed at Motorola's Advanced Products Research and Development Laboratory. Even though the author has participated in the research efforts of numerous engineers,[116,117,118,119,120,121,122,123,124,125,126,127,128,129,130,131,132] the scope of this dissertation will be limited to the investigations in which this author was the primary investigator.[123,124,125,126,127,128,129,130,131,132] Thus, in the spirit of a Ph.D., this author will primarily present research in which he was responsible for the experiment definition and research direction. In addition, there are instances where the author contributed to other research projects and times where colleagues provided information or data to the author. It is required that small amounts of these interactions are included in this dissertation for the dissertation to be fully coherent and complete. This is an unavoidable consequence of performing collaborative industrial research. However, even with this collaborative approach, the author still established proficiency and expertise in focused methods and topics, while at the same time learning how to define, direct, and conclude research initiatives. In this regard, this graduate student experience should not be terribly different from that of a traditional student.

The primary experimental techniques employed for these studies will be discussed in Chapter 2. This includes a description of the two primary deposition systems employed in this research. For the HfO_2 gate dielectric investigations a metal organic chemical vapor deposition system (Sec. 2.2) was used and for the various metal gate electrodes a physical deposition system was employed (Sec. 2.3). Another section will discuss the equipment used to probe the electrical and physical properties of the materials in this investigation will be provided (Sec 2.4).

Chapter 3 focuses on the metal organic chemical vapor deposition of HfO_2 gate dielectrics using tetrakis diethylamino hafnium (TDEAH) precursor. The physical properties of the gate oxide at various growth conditions are investigated. Electrical measurements of the dielectrics reveal the desired growth conditions and physical properties that are desired to produce a high quality gate dielectric.

Chapter 4 investigates the materials characteristics of several metal gate electrodes and their thermal stability in contact with HfO_2 gate dielectrics. Since this is the first time the thermal properties of many of the metal gate electrodes have been studied on HfO_2 these investigations have helped establish a selection criterion for metal gate electrodes in contact with HfO_2. The work functions of multiple electrodes are investigated to determine whether they are potential metal gate electrode candidates on HfO_2.

The first two chapters link nicely into Chapter 5, which discusses a phenomena that occurs at the metal-dielectric interface called Fermi level pinning. The investigations in Chapter 5 will illustrate why the effective work function of a metal in contact with a dielectric is not the same as its vacuum work function. In addition, this chapter investigates the intrinsic and extrinsic origins of Fermi level pinning, and how its impact might be minimized to successfully implement these new materials into advanced MOSFETs.

Chapter 2: Experimental

2.1 INTRODUCTION

This research utilized a variety of film growth and film characterization equipment. The author had primary responsibility for the two thin film deposition techniques described below. The film deposition equipment includes a metal organic chemical vapor deposition (MOCVD) system for HfO_2 deposition and a physical vapor deposition (PVD) system for metal gate electrode deposition. The author developed the dielectric and metal processes discussed in this research. To develop the processes experiments were developed that utilized a variety of analytical tools to study various film properties. The author determined which analytical techniques were required to properly characterize the deposited materials and also which experiments were required to understand the behavior of the MOCVD and PVD processes used to deposit the films. A variety of analytical tools were employed and the author typically coordinated the analyses with an individual who is considered an expert in the given analytical technique. Additionally, some limited electrical characterization was performed in these studies. The author performed the majority of the electrical characterization discussed in this dissertation. However, in a few instances the measurements were performed by colleagues. Section 2.2 will discuss the MOCVD system and Section 2.3 will discuss the PVD system, Section 2.4 will briefly discuss the electrical characterization hardware and some of the analytical tools employed for film characterization.

2.2 METAL ORGANIC CHEMICAL VAPOR DEPOSITION SYSTEM

A MOCVD system capable of depositing on 200mm wafers was used for the deposition of HfO_2 films studied in this research. This reactor consists of three primary components: 1.) the liquid delivery system (LDS), 2.) the direct liquid injection (DLI) system, and 3.) the reaction chamber. The MOCVD reactor is mounted on a platform consisting of two load locks that pump down (up) from atmosphere (base pressure) for loading (unloading) wafers and a transfer chamber with a robot that moves wafers between the load locks and the process chambers. The transfer chamber has a base pressure of ~$1x10^{-7}$ Torr.

The liquid delivery system (LDS) contains four ampoules. Two of the ampoules contain liquid process chemicals and two of the ampoules contain liquid solvents. The solvents are used to purge process chemical from the delivery lines. All gas lines are ¼" stainless steel lines with VCR connections. All chemical lines are 1/8" stainless steel lines with VCR connections. The ampoules are 1.8 liters in volume. Each ampoule has an inlet and an outlet tube. The inlet line does not dip into the process chemical. Argon gas flows into the inlet line to create an over pressure above the liquid precursor. The outlet line dips into the process chemical. When valves are opened appropriately, the over pressure created by the argon gas pushes the process chemical up and into the outlet line. Liquid precursor is then carried outside of the LDS to the DLI cabinet. (Fig. 2.1)

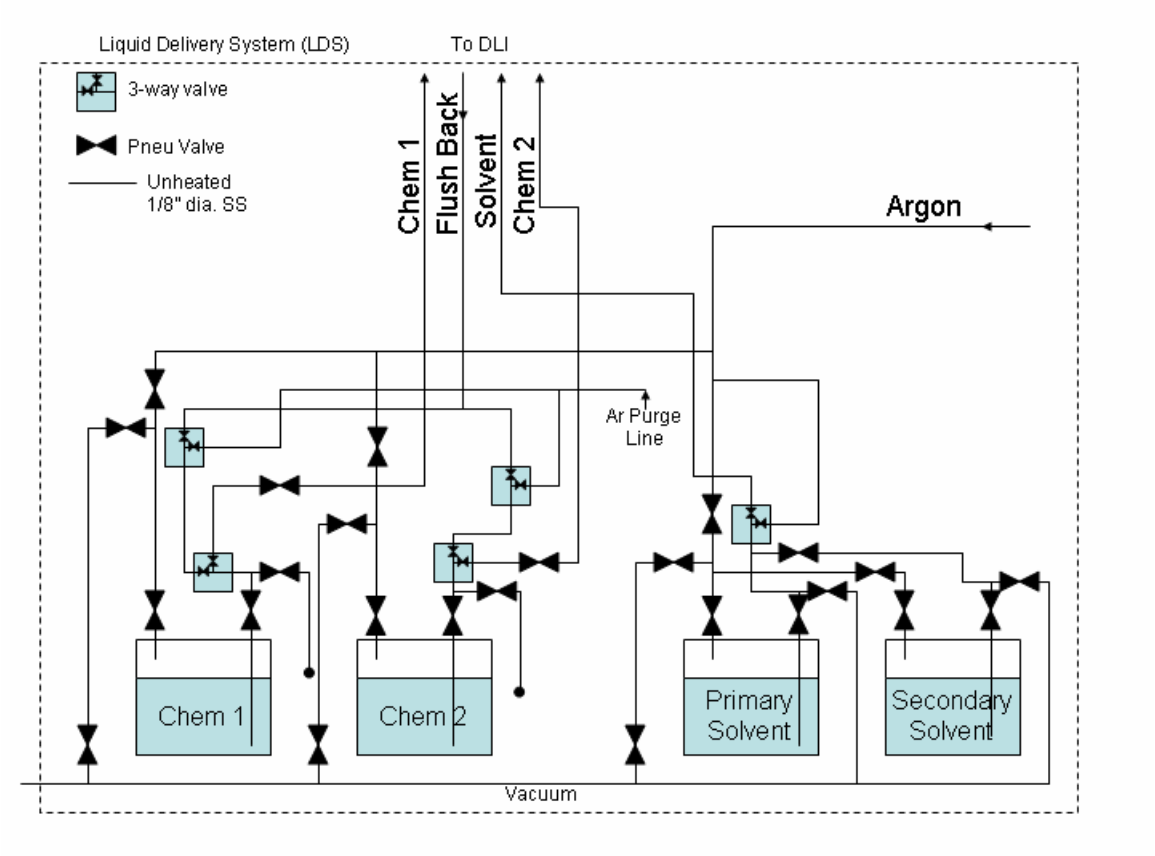

Figure 2.1: Schematic of the liquid delivery system.

The DLI system is mounted directly onto the side of the chamber. The DLI system consists of three liquid flow controllers, stainless steel precursor mixing blocks, and a heated vaporizer unit. The liquid flow controllers provide independent control over the flow rate of the two liquid precursors and one solvent so that variable composition films can be deposited. After the precursor is metered through the liquid flow controller it enters a series of mixing blocks. Upon entering the mixing block manifold the two liquid chemicals merge into one delivery tube. Since the liquid precursors are mixed in the liquid phase it is necessary to use precursors that have chemical compatibility with each other. After being mixed the precursors enter a 0.010 inch inside diameter Teflon tube that delivers the precursor into the heated vaporizer unit. The vaporizer consists of a porous aluminum frit, whose temperature is controlled or optimized at or above the boiling point of the precursor and below the decomposition point of the precursor. Two argon gas lines mix with the precursor near the vaporizer. The first line (argon-A) mixes with the precursor immediately before the vaporizer. The second line (argon-B) mixes with the chemical inside the vaporizer. After exiting the vaporizer, the gas lines increase to 1" in diameter and they are heated with an increasing downstream temperature gradient to avoid precursor condensation. A heated final valve diverts precursor either to the by-pass or to the chamber. In typical operation, a steady flow of precursor is established through the vaporizer and is diverted towards the by-pass. Once a steady precursor flow has been established the final valve opens to deliver precursor to the reaction chamber.

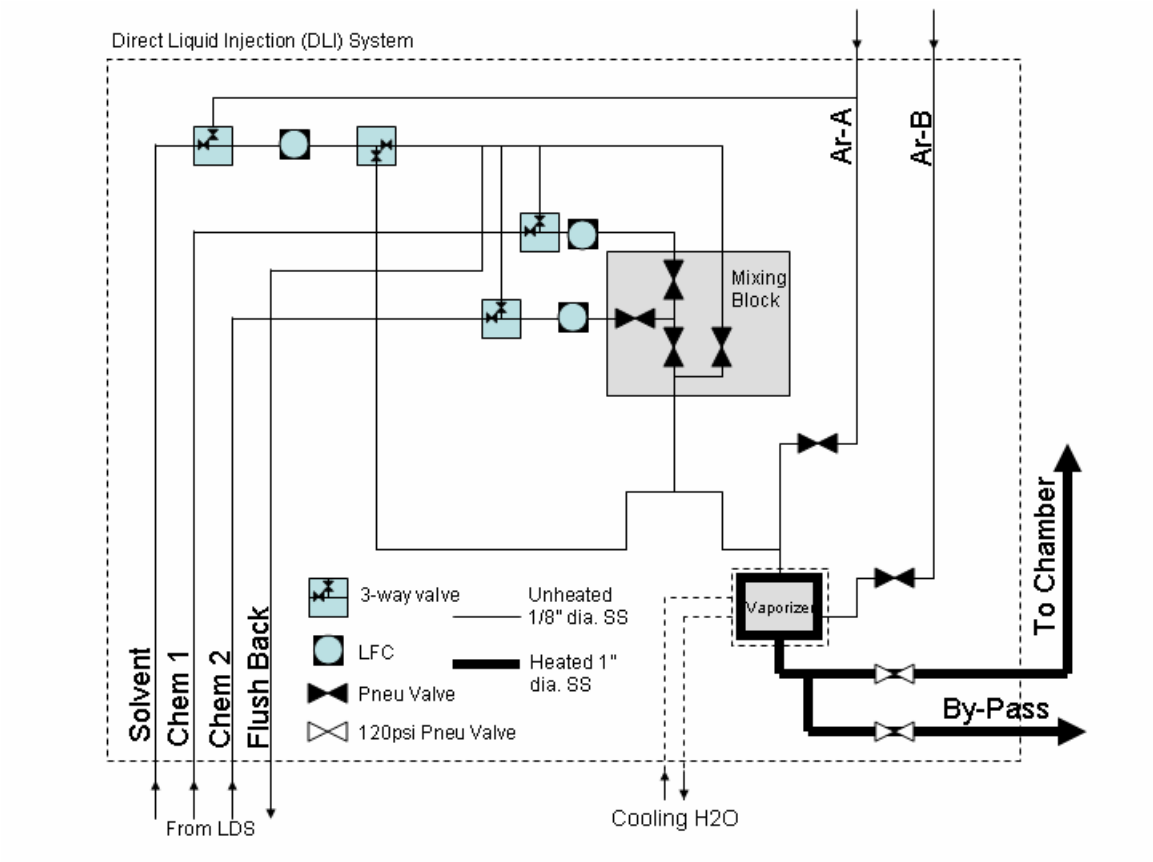

Figure 2.2: Schematic of the direct liquid injection system.

The reaction chamber contains a ceramic heater with a temperature range of ~300°C to ~700°C. A heat exchanger unit cycles ethylene glycol through the chamber walls to keep them near 60°C. The precursor enters the reactor from the bottom of the chamber. It is delivered through a tube in the chamber wall to the top of the reactor where it enters the chamber through a heated shower head designed for uniform distribution of precursor flow to the wafer surface. Process gases such as Ar, N_2, O_2, and N_2O also enter through the shower head.

Tetrakis diethylamino hafnium (TDEAH) (Fig. 2.3) was the precursor selected for HfO_2 film growth in this reactor. TDEAH was selected because it is a low viscosity liquid precursor that can be delivered using a direct liquid injection system. TDEAH is also completely compatible with tetrakis dimethylamino silicon (TDMAS) which makes this precursor combination a good choice for the deposition of hafnium silicate films. The vapor pressure curve as a function of temperature is also provided for TDEAH. (Fig. 2.4)

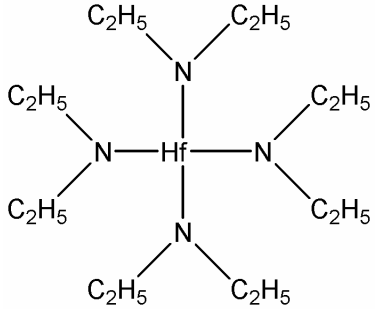

Figure 2.3: TDEAH ($Hf[N(C_2H_5)_2]_4$) precursor was used for the deposition of HfO_2 dielectric films

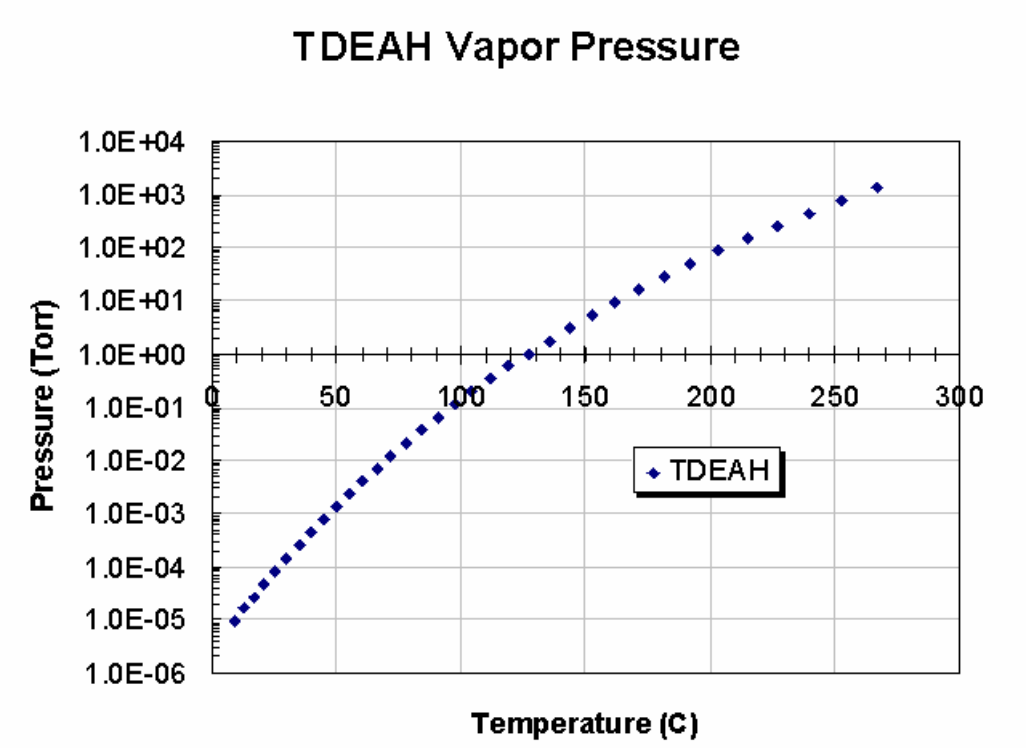

Figure 2.4: Vapor pressure versus temperature curve for TDEAH precursor.

Process optimization was performed to achieve repeatable depositions. This entailed screening experiments that evaluated the TDEAH, O_2, process Ar, Ar-A, Ar-B, pressure, heater temperature, and vaporizer (and gas line) temperatures. These experiments revealed that the process was most sensitive to the vaporizer (and gas line) temperatures and the heater temperature. The vaporizer temperature was set near the boiling point of TDEAH which is 125°C at 0.5 mm Hg and well below the thermal decomposition temperature of 200°C. Experiments were carried out at three different heater temperatures (325°C, 485°C, and 550°C). The deposition rate is observed to decrease with increasing temperature from 2.2Å/s to 1.6Å/s to 1.4Å/s for 325°C, 485°C, and 550°C heater temperatures respectively (Fig. 2.5). It is possible that this is due to undesirable decomposition of TDEAH on the shower head or side walls of the chamber whose temperatures are observed to increase when the heater temperature increases.

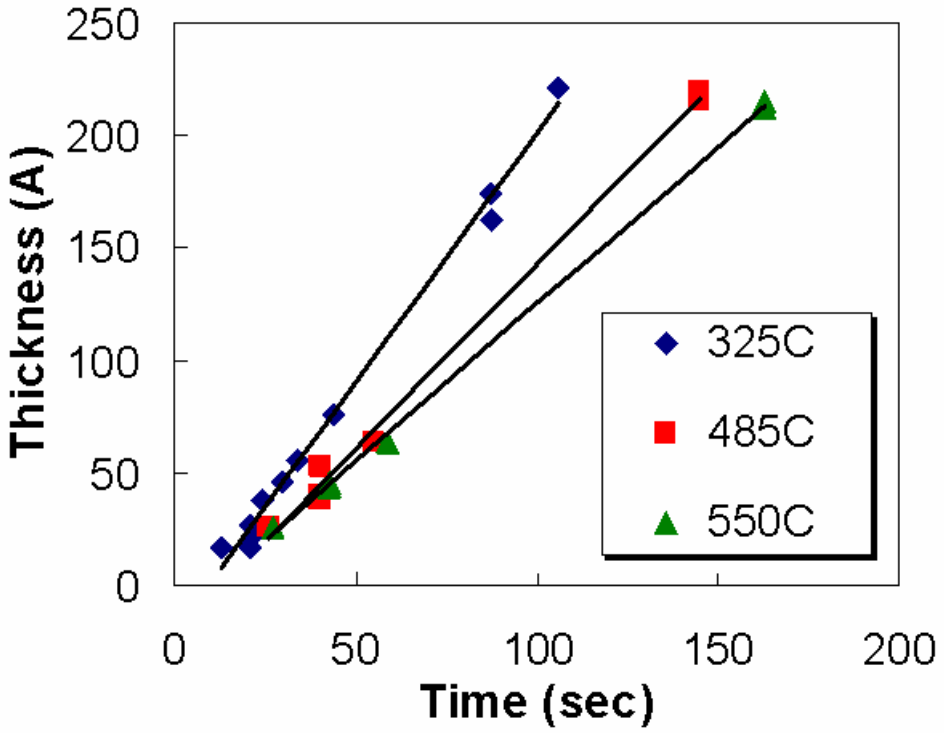

Figure 2.5: Plot of time vs. thickness for HfO_2 films deposited with TDEAH precursor. Deposition rate decreases with increasing temperature.

2.3 PHYSICAL VAPOR DEPOSITION SYSTEM

A PVD system capable of processing 200mm wafers was used to deposit the metal gate electrodes. This physical vapor deposition system has load locks and transfer chambers similar to those used on the MOCVD system. The base pressure of the transfer chamber is ~1×10^{-8} Torr.

The reaction chambers are pumped to base pressures of ~1×10^{-8} Torr. These reactors are magnetron sputtering systems. These reactors consist of a heated wafer pedestal, consumable shield kits to avoid undesirable sputtering on the chamber side walls, and a metal target which is typically solder bonded to a copper backing plate. The backside of the target backing plate is cooled with de-ionized water. Behind the backing plate, and submersed in the de-ionized water, is a rotating magnet assembly. The magnet assembly helps sustain the plasma by increasing the electron path length to increase the probability of collisions. This allows the process to be operated at lower target voltages and lower pressures. The target backing plate is biased with a direct current (DC) power supply. Detailed descriptions of the DC magnetron sputtering process are available.[133]

Reactive sputtering approaches were used for the sputtering of nitride films. This entails sputtering from a metal target (ie. Ti, Ta, etc.) in the presence of argon and nitrogen gas. Titanium nitride is the classic example of reactive sputtering because only pure titanium, the mono-nitride (TiN), and mixtures of the two are formed during the sputtering process. In reactive sputtering a balance exists between deposition rate and N_2/Ar ratio. Nitrogen adsorbs on the target surface when it is introduced into the chamber. When the argon ions bombard the target surface both Ti and N species are ejected off the target towards the wafer. With only small additions of nitrogen, nitrogen is being sputtered off the target surface faster than its sticking rate to the target. Thus,

with increasing nitrogen flow, the nitrogen composition in the film will increase steadily. However, with large additions of nitrogen the sticking rate of nitrogen on the target surface is faster than the nitrogen sputtering rate. This is termed target "poisoning". Since the ion bombardment at higher flow rates goes into sputtering the adsorbed nitrogen the deposition rate typically drops, the resistance of the films typically increases, and the target voltage typically increases. The increase in target voltage can occur when the presence of the more resistive TiN phase forms on the target surface. This increases the chamber impedance resulting in the increased target voltage for a given sputtering power. Deposited films with the rock-salt structure of TiN are typically obtained at N_2 gas flow rates higher than where the transition from a low to a high resistivity film is observed. (Fig. 2.6) The sheet rho saturates at higher N_2/Ar ratios because no phases of TiN_x where $x > 1$ can be formed. Most of the excess nitrogen is pumped from the reactor, although it is possible to create metastable nitrogen rich films. Titanium nitride is a well characterized and well understood sputter process. The titanium nitride example below is an example of the classic target poisoning curve.

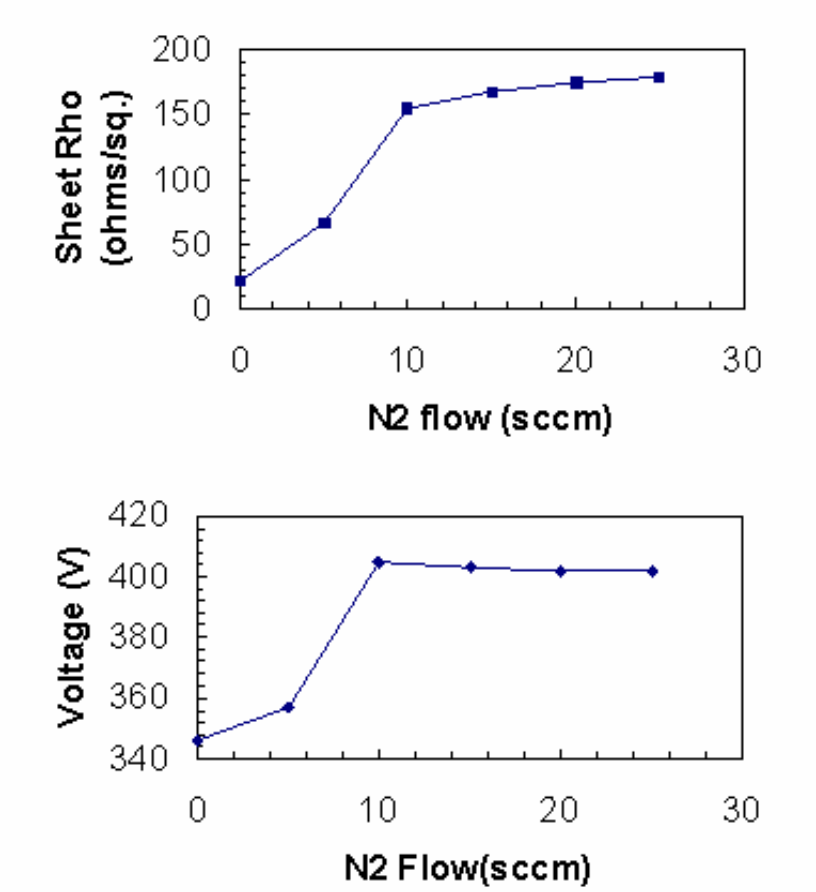

Figure 2.6: Representative behavior for the sheet rho of TiN_x films and the target voltage during the reactive sputtering of TiN films.

More complex materials systems exist where the target poisoning curve does not have this ideal behavior. In the reactive sputtering of some materials multiple minima/maxima are observed in curves of resistivity versus the percent of reactive gas. This is often due to the presence of multiple phases. For example, in the reactive sputtering of TaN_x, slight additions of nitrogen will stabilize the body-centered-cubic phase of tantalum. This phase has a lower resistivity than the β tantalum phase that forms when no nitrogen is present. Additionally, two tantalum nitride (Ta_2N and TaN) and even a very high resistive phase (possibly Ta_3N_5) are encountered during the reactive sputtering of TaN_x. Extensive film and materials characterization is required to understand what phases are present at any given composition. Reactive sputtering has been used to form oxide (O_2/Ar), nitrides (N_2/Ar) and carbides (C_xH_{2x+2}/Ar).

2.4 ELECTRICAL TEST EQUIPMENT AND PHYSICAL ANALYSIS TECHNIQUES

Electrical test was performed using the HP 4194A Impedance/Gain-Phase Analyzer and the HP 4156B Precision Semiconductor Parameter Analyzer. A range of physical analysis techniques have been employed during these studies. These include X-ray diffraction (XRD),[134] X-ray photoelectron spectroscopy (XPS),[135,136,137] Auger electron spectroscopy (AES), Rutherford backscattering spectroscopy (RBS),[138,139] Raman spectroscopy, ultra-violet spectroscopic ellipsometry (SE),[140] secondary ion mass spectroscopy (SIMS),[141] transmission electron microscopy (TEM),[142] and ultra-violet photoelectron spectroscopy (UPS). Since these techniques are not the focus of this dissertation, but were used to generate supporting data, each one will not be discussed in detail. Some references have been provided for additional details on these analysis techniques.

Chapter 3: HfO_2 Gate Dielectrics Deposited via Tetrakis Diethylamino Hafnium

3.1 ABSTRACT

HfO_2 films deposited via tetrakis diethylamino hafnium (TDEAH) precursor using MOCVD (Metal Organic Chemical Vapor Deposition) are presented. TDEAH is a promising precursor candidate for the deposition of high permittivity gate dielectrics. The impact of process and annealing conditions on the physical and electrical properties of the film are reported. Deposition and annealing temperatures influence the microstructure, density, and impurity levels of TDEAH HfO_2 films. Spectroscopic ellipsometry shows that film microstructure manifests itself in the optical properties of the film, particularly in the presence of a band edge related feature at 5.8eV. An impurity analysis using AES, SIMS, and Raman Spectroscopy, indicates that carbon impurities from the precursor exist as clusters within the HfO_2 dielectric. The impact of deposition temperature and annealing temperature on the capacitance vs. voltage and current Density vs. voltage characteristics of platinum gated capacitors is studied. Correlation of physical film properties with the capacitance and leakage behavior of the TDEAH HfO_2 films indicates that impurities, in the form of carbon clusters, and low HfO_2 film density are detrimental to the electrical performance of the gate dielectric.

3.2 INTRODUCTION

As the smallest feature size on a microprocessor approach 50nm, the primary dielectric layer in the field effect transistor, referred to as the gate dielectric or gate oxide, will thin to below 15 Å. Around this thickness electrical leakage current through the dielectric becomes excessive and is expected to cause problems due to either high power

dissipation or circuit reliability.[143] One solution to this problem is to replace SiO_2 dielectrics with higher permittivity dielectrics. A higher permittivity dielectric can be thicker and still achieve the same capacitance as a thinner SiO_2 dielectric. The starting point for identifying possible replacements for SiO_2 dielectrics is to evaluate their thermal stability in direct contact with silicon. Reactions between the high permittivity dielectric and the silicon substrate or electrode are undesirable. Extensive thermodynamic calculations have been performed by Hubbard and Schlom,[144] identifying numerous binary and ternary oxides that are candidate materials. Some of the binary oxides that are leading contenders for replacing SiO_2 include: ZrO_2, HfO_2, Y_2O_3, and Al_2O_3. In addition, there are numerous ternary (or mixed) oxides that have also been predicted, or experimentally determined, to be stable in contact with silicon. In general, the class IIIB and IVB oxides tend to be the most thermodynamically stable oxides for potential use in integrated circuit manufacturing. Doping the IIIB and IVB oxides with Al_2O_3 or SiO_2 increases the crystallization temperature. Such amorphous dielectrics are desirable because grain boundaries enhance diffusion of dopants from the electrode to the substrate and possibly contribute to electrical leakage. On the other hand, doping with Al_2O_3 and SiO_2 will also lower the permittivity of the resultant dielectric. There are many other considerations associated with the selection of high permittivity gate dielectrics.[145] This chapter provides insight into the physical and electrical properties of HfO_2 films deposited with tetrakis diethylamino hafnium (TDEAH) precursor via MOCVD. In this work, the physical analysis has been correlated to the capacitance and leakage properties of the dielectrics. This work shows that increasing the deposition temperature of TDEAH HfO_2 films has a significant impact on the leakage characteristics of the dielectric. An explanation of the responsible physical properties is presented.

3.3 EXPERIMENT

Tetrakis diethylamino hafnium (TDEAH) is one of many candidate precursors for the deposition of hafnium oxide thin films grown via MOCVD. Reports of HfO_2 deposition using a wide array of organometallic precursors exist.[146] There are five classes of precursors typically used for MOCVD of Group IVB materials. The five classes, based upon the ligands include: halides, alkoxides, beta-diketonates, nitrates, and alkylamides. Compounds with a mixture of ligands have also been synthesized. These compounds capitalize on the most desirable properties of each ligand type. TDEAH is an alkylamide, and one of the most promising precursors for implementation in a manufacturing environment. TDEAH is a low viscosity, liquid precursor that can be repeatably delivered using a direct liquid injection system. TDEAH is also completely compatible with TDMAS (tetrakis dimethylamino silicon). This combination of precursors can be used to deposit hafnium silicate films, which are currently of interest because they posses higher crystallization temperatures than hafnium oxide films.

A cold walled CVD reactor was used for these depositions. The reaction chamber is outfitted with a direct liquid injection (DLI) delivery system. The liquid precursor is metered through the delivery lines to a vaporizing unit mounted on the side of the chamber. An argon dilution gas (Ar-A) enters the precursor delivery lines immediately before the vaporizer unit. At the vaporizer, an argon carrier gas (Ar-B) is introduced at the point of vaporization to carry the chemical the short distance from the vaporizer unit to the shower head. Additional process gases such as O_2 and Ar are mixed with the vaporized precursor just before entering the shower head. The chamber pressure and flow rates of all species were held constant in this study. Calculations based on the flow rates of each species indicate that approximately 800 O_2 molecules per TDEAH molecule enter the reaction chamber. Thus, the process operates in an excess of oxygen.

The silicon substrates used in this experiment were n-type with a resistivity of 10 ohm-cm. The substrates were prepared for deposition with an HF (hydrofluoric acid) wet clean immediately prior to deposition. Films were deposited at three deposition temperatures (325 °C, 485 °C, and 550 °C). Films with target thickness of 30 Å, 50 Å, 70 Å, and 200 Å were grown at each deposition temperature. Every wafer was cleaved into four pieces with each piece getting a different anneal condition. The anneal splits included no anneal, 700 °C - 60 sec - N_2, 800 °C - 60 sec - N_2, and 900 °C - 60 sec - N_2. Shadow masked platinum capacitors were deposited on the 30 Å, 50 Å, and 70 Å samples for capacitance-voltage (C-V) and current density – voltage (J-V) measurements. Unless specified, the 200 Å films were used for the majority of the physical characterization.

3.4 PHYSICAL CHARACTERIZATION RESULTS AND DISCUSSION

HfO_2 films deposited with TDEAH precursor were analyzed extensively for the effects of deposition and post-annealing temperature on film impurities, microstructure, band-gap, and density. Deposition and annealing temperature influence the film impurities and microstructure of the film. The film microstructure, and possibly the film impurities, manifests in the optical properties, and band-edge related features.

Microstructure Analysis

HfO_2 films were evaluated with XRD, TEM, and transmission electron diffraction (TED) techniques to evaluate film microstructure. Films deposited at 325 °C were amorphous as deposited, but crystallized into a poly-crystalline tetragonal phase upon annealing (Fig. 3.1). Note the featureless diffraction data for the as-deposited samples compared to the annealed samples that exhibit strong reflections from a tetragonal phase

of HfO_2. The amorphous HfO_2 films de-vitrify easily,[147] and transform into a poly-crystalline phase even at the lowest annealing temperature used in this study of 700 °C. XRD data indicate that the HfO_2 grain size is approximately 100 Å for a 200 Å thick film. Transmission electron microscopy of the TDEAH HfO_2 films reveals an amorphous structure as deposited that crystallizes after annealing (Fig. 3.2 and 3.3). Although the film anneal is in a N_2 ambient, a significant growth of the interfacial layer results after annealing. Anneals on these samples were performed at atmospheric pressure, and a small partial pressure of oxygen in the RTA (rapid thermal annealer) may be responsible for the ~9 Å of interfacial layer growth. It is also speculated that oxygen from the HfO_2 might be activated by high temperature annealing for out-diffusion and subsequent interfacial layer growth.

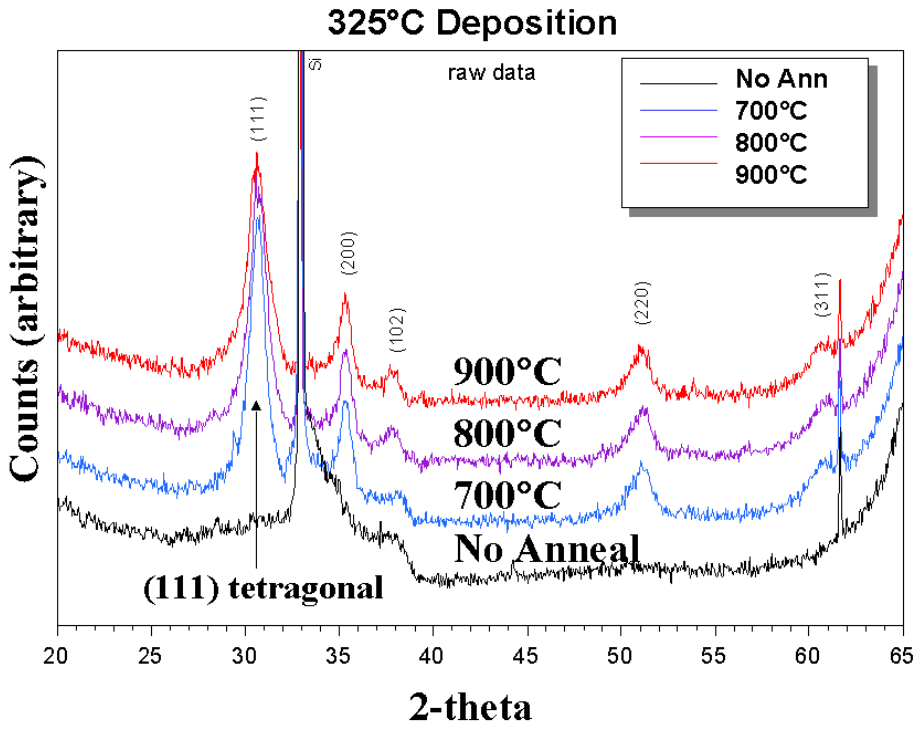

Figure 3.1: Diffraction data for TDEAH HfO_2 deposited at 325°C.

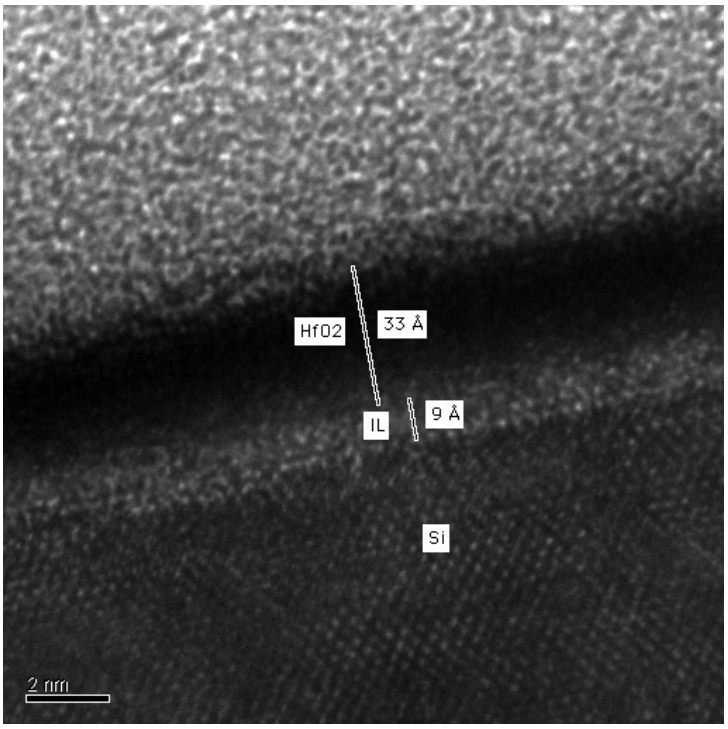

Figure 3.2: TEM of TDEAH HfO_2, 325 °C deposition, no anneal

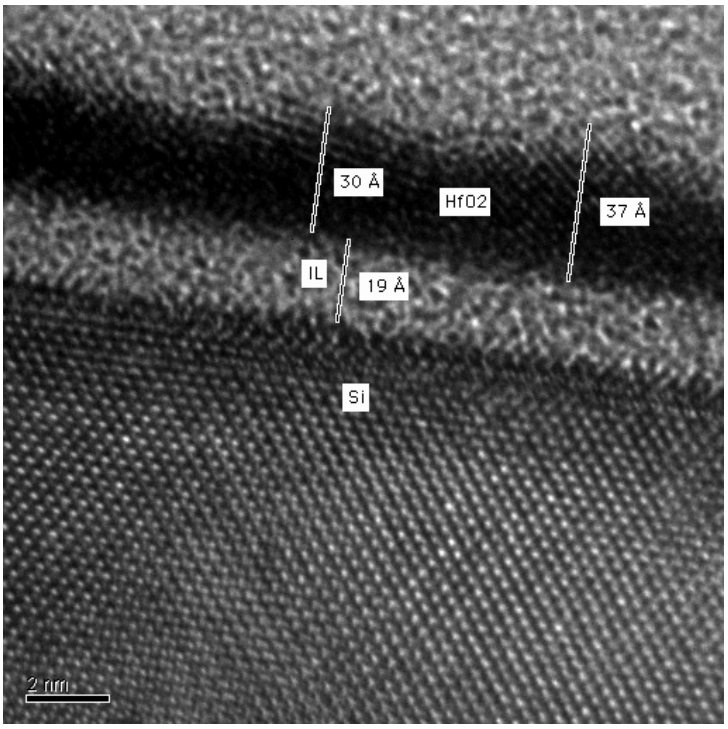

Figure 3.3: TEM of TDEAH HfO_2, 325°C deposition, 900 °C-60 sec-N_2

The films deposited at 485 ºC are a mixed phase of tetragonal and monoclinic HfO_2 as deposited. These films convert from the tetragonal to a mostly monoclinic, or baddeleyte, phase upon annealing. (Fig. 3.4) The reflection at $2\theta = 30.02°$, provides evidence for the existence of the tetragonal phase in the as-deposited samples. XRD data indicates the grain size is approximately 150 Å for a 200 Å film, a 50 Å increase in diameter from the films deposited at 325 ºC. The transmission electron micrographs of the TDEAH HfO_2 films deposited at 485 ºC show the poly-crystalline microstructure for both the as-deposited and the annealed conditions. The interfacial layer is observed to increase by about 6 Å after the 900 ºC-60sec-N_2 anneal.

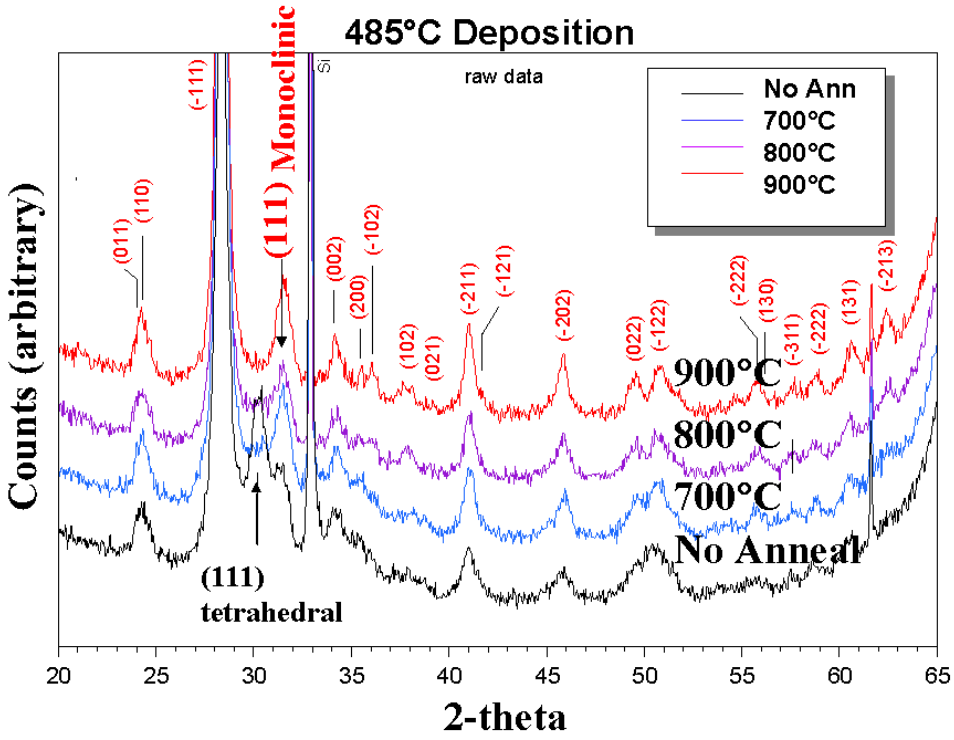

Figure 3.4: Diffraction data for TDEAH HfO_2 deposited at 485 °C

At 550 ºC, the diffraction data indicate a poly-crystalline, (-111) textured, monoclinic microstructure as deposited and after anneal (Fig. 3.5). The grain size is approximately 160 Å for 200 Å films. Transmission electron micrographs of the TDEAH HfO_2 films deposited at 550 ºC show a polycrystalline HfO_2 layer for both as-deposited and annealed samples (Fig. 3.6 and 3.7). The interfacial layer increases from 15 Å to 21 Å after the 900 ºC-60s-N_2 anneal.

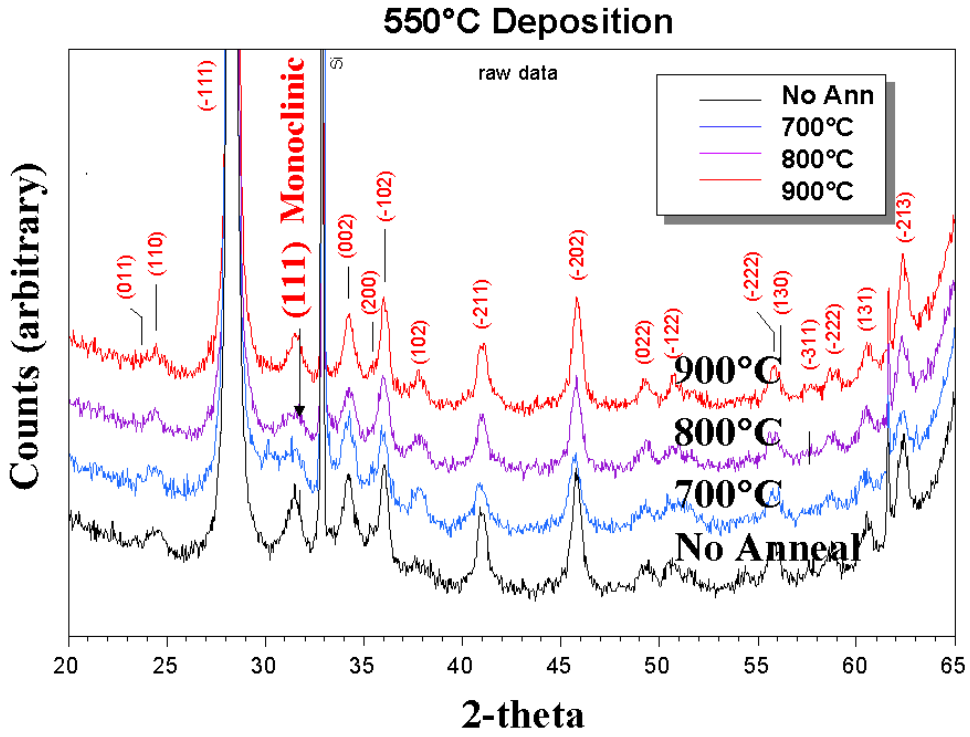

Figure 3.5: Diffraction data for TDEAH HfO_2 deposited at 550 ºC

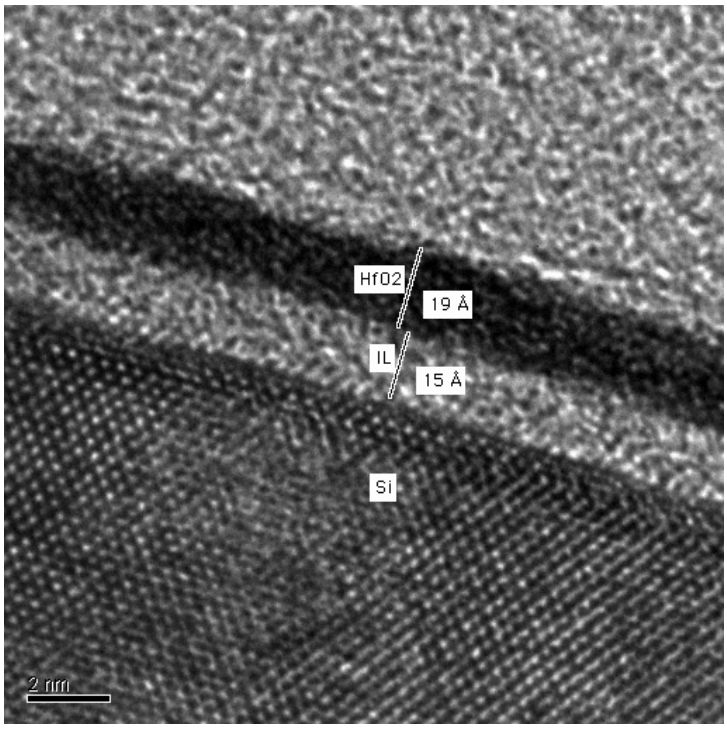

Figure 3.6: TEM of TDEAH HfO_2, 550°C deposition, no anneal

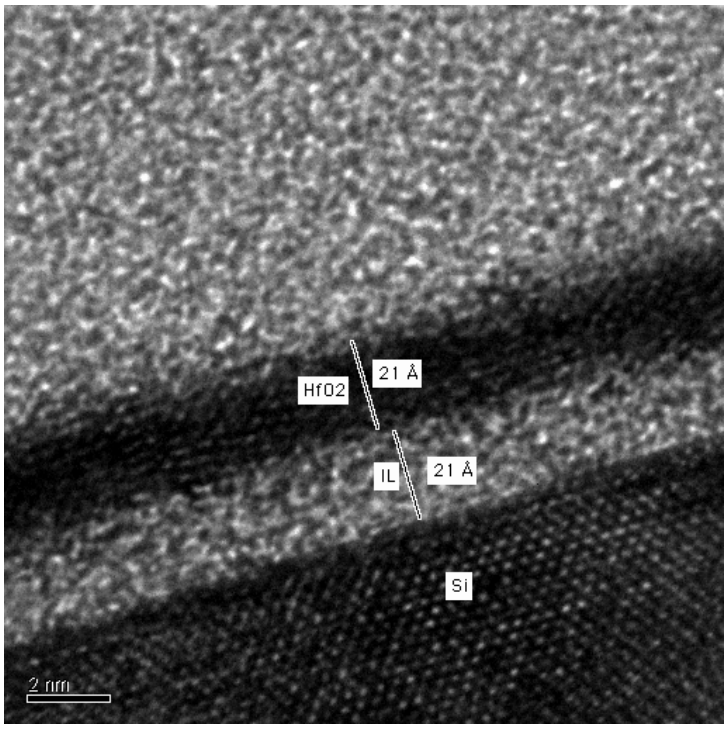

Figure 3.7: TEM of TDEAH HfO_2, 550°C Deposition, 900°C-60 sec-N_2

In summary, the microstructure analysis indicates TDEAH films deposited at 325ºC were amorphous as deposited, crystallizing to a tetragonal phase upon annealing. At 485 ºC, the films were a mixed tetragonal/monoclinic phase, with a transition to a purely monoclinic phase with subsequent annealing. At the highest deposition temperature of 550 ºC, the TDEAH HfO_2 films were monoclinic as deposited and after annealing. It has been noted that at lower deposition temperatures (or lower thermal processing conditions), higher temperature phases of HfO_2 films predominate. Increasing the deposition temperatures and the annealing temperatures, results in a transition to the lower temperature (monoclinic) phase of HfO_2. The monoclinic phase of HfO_2 is stable below ~1670 °C.[150] A transition from the tetragonal phase of HfO_2 to the monoclinic phase of HfO_2 with increasing thermal budget is observed in this study. The formation of metastable ZrO_2 and HfO_2 polymorphs at low growth temperatures, with a transition to lower temperature phases of ZrO_2 and HfO_2 at higher growth temperatures has previously been reported using both metal organic chemical vapor deposition and atomic layer deposition.[148,149] The stability of higher temperature, metastable polymorphs is attributed to an additional surface energy factor that is relatively large in smaller grains. Smaller grain diameters for films deposited at lower substrate temperatures are also observed in this study. It is acknowledged that the presence of metastable HfO_2 polymorphs at lower deposition temperatures may also be related to carbon impurities, deposition rate, or the kinetic growth regime of the film, all of which are strongly related to the deposition temperature.

TEM reveals a significant interfacial layer growth for all the annealed samples. The amorphous interfacial layer grows 6-9 Å after annealing. The most likely cause for the interfacial layer growth is the presence of an oxygen partial pressure during the atmospheric N_2 anneals. An alternative cause of the interfacial layer growth is due to an

out-diffusion of atomic oxygen from the as deposited TDEAH HfO_2 films. The equilibrium HfO_2 phase diagram indicates that the HfO_2 phase can remain stable with up to 3 at.% sub-stoichiometric oxygen concentration.[150] Therefore, it may be possible that through oxygen vacancy formation in HfO_2, oxygen is available to react with the silicon substrate. This explanation contradicts a more recent study that claims that since HfO_2 has a higher affinity for oxygen than SiO_2, the SiO_2 interfacial layer can be reduced at temperatures well below that required for SiO(g) evolution.[151] However, if the films are super-saturated with oxygen, so that the oxygen vacancy concentration is smaller than its equilibrium concentration, the origin of the interfacial layer growth may be excess oxygen from the HfO_2. Since the reactor ambient consisted of approximately 800 times more oxygen molecules than TDEAH molecules it is possible that a super-saturation of oxygen was created in the as-deposited film. Previously, HfO_2 films deposited using $Hf(NO_3)_4$ were found to have an as-deposited stoichiometry with RBS of $HfO_{2.2}$ to $HfO_{2.4}$.[146,152] Therefore, in oxygen-rich HfO_2, the oxygen might out-diffuse upon annealing to react and form SiO_2 at the silicon interface.

Impurity Analysis

Auger electron spectroscopy, SIMS, and Raman spectroscopy were performed on all HfO_2 films to analyze the impurity concentrations at various deposition and annealing conditions. AES depth profiling shows detectable carbon and nitrogen impurities in HfO_2 films deposited at 325 ºC. (Fig. 3.8) The alkylamide precursor, $Hf\text{-}(N\text{-}(C_2H_5)_2)_4$, is the source of both the nitrogen and carbon impurities. Post-annealing has minimal effect on eliminating the carbon impurities in the HfO_2 films. AES depth profiles for films deposited at 485 ºC and 550 ºC show a dramatic reduction in the carbon and nitrogen impurity levels compared to the 325 ºC samples. At the 550 ºC deposition condition with

a 900 ºC-60s-N_2 anneal, there appears to be some silicon diffusion into the HfO_2 film from the substrate or the poly-Si capping layer. This is shown by a slight increase of silicon in the bulk of the HfO_2. (Fig. 3.8)

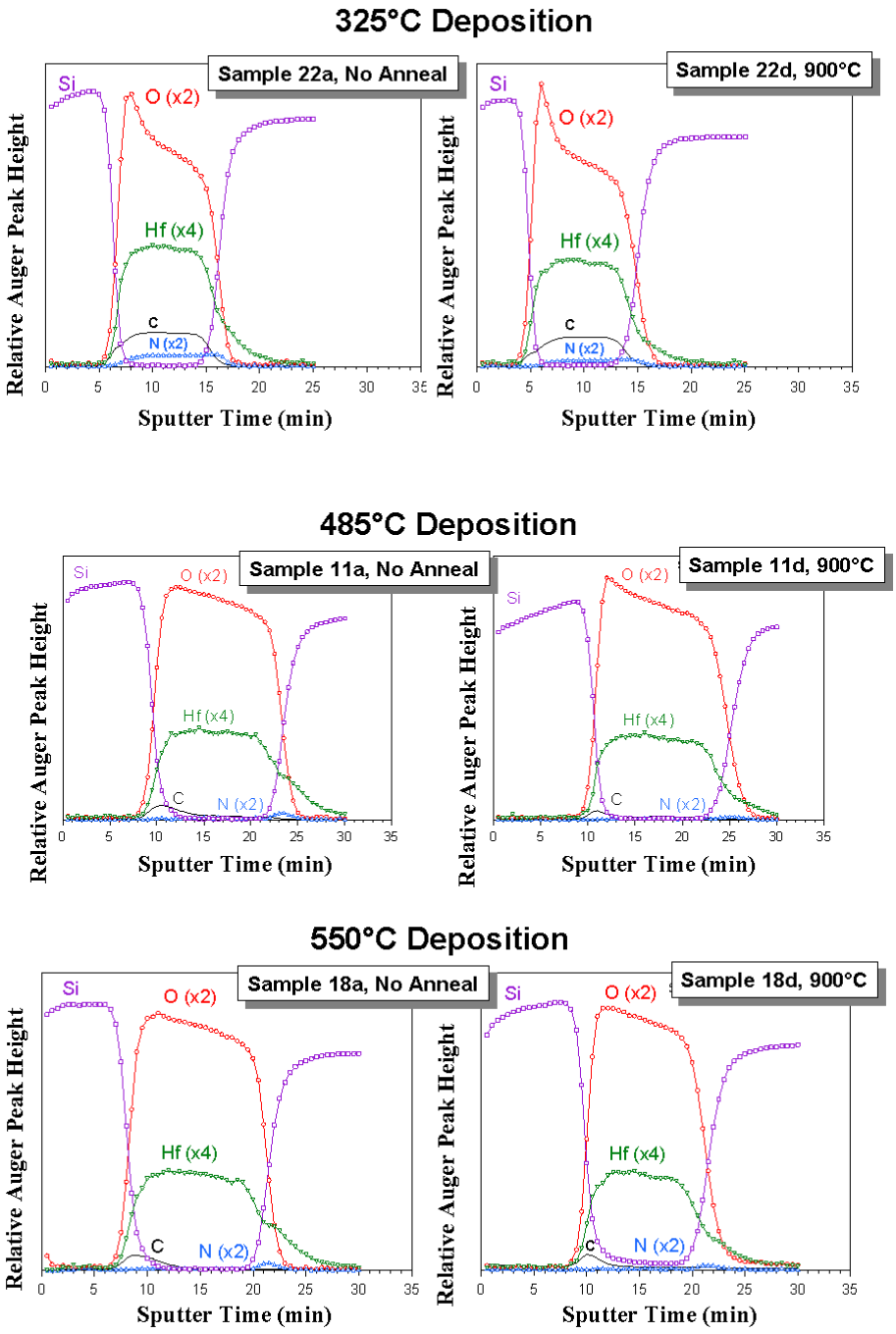

Figure 3.8: Auger Electron Spectroscopy depth profiles for TDEAH HfO_2 films deposited at 325 ºC, 485 ºC, and 550 ºC. As deposited and annealed (900 ºC-60s-N_2) conditions are shown.

Secondary ion mass spectroscopy (SIMS) provided enhanced resolution for the carbon impurity measurement. (Fig. 3.9) The SIMS depth profiles show a distinct reduction in the carbon impurity levels with increasing deposition temperature. SIMS depth profiles also indicate that post-annealing has minimal effect on reducing the film impurities. The samples deposited at 550 ºC have a non-uniform composition gradient of carbon impurities compared to samples deposited at 325 ºC and 485 ºC. It is possible that the non-uniform carbon depth profile in the 550ºC samples might be due to the presence of adventitious carbon from ambient exposure. It can be reasoned that during the SIMS depth profiling ion bombardment of the surface carbon into HfO_2 from is responsible for the decreasing carbon tail into the bulk of the HfO_2.

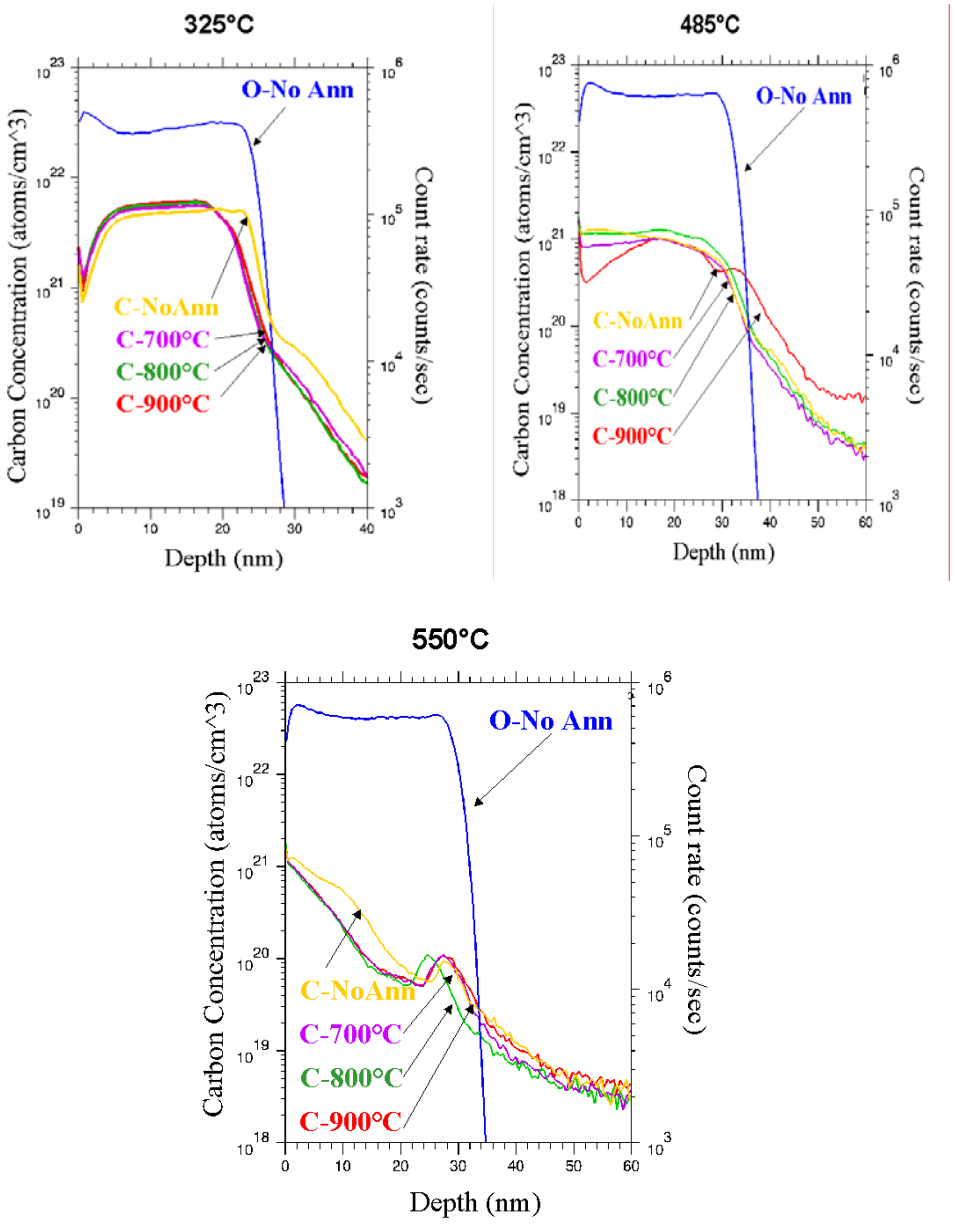

Figure 3.9: SIMS depth profiles for TDEAH HfO_2 films deposited at 325 ºC, 485 ºC, and 550 ºC.

Raman spectroscopy on as deposited and annealed samples at each deposition temperature was used to analyze the local bonding arrangement of the carbon impurities. (Fig. 3.10) The data revealed two broad Raman peaks at 1400 and 1600 cm^{-1}, corresponding to diamond-like (sp^3) and graphite-like (sp^2) bonded carbon clusters, in the 900 ºC - 60sec - N_2 annealed films deposited at lower temperatures (325ºC and 485ºC). Contrary to the SIMS depth profiles, analysis of the as-deposited, 325 ºC film revealed no amorphous carbon with Raman spectroscopy. This indicates that in the as-deposited sample the carbon detected by SIMS might be bound to hydrogen, and not as an amorphous carbon cluster. Subsequent annealing of films deposited at 325 ºC, results in the formation of amorphous carbon clusters detected by Raman scattering. For the 485ºC films, amorphous carbon is detected in both the as-deposited and annealed films. The peak intensity for the film deposited at 485 ºC is reduced compared to the annealed samples deposited at 325 ºC. Raman spectroscopy does not detect carbon in any of the 550 ºC films.

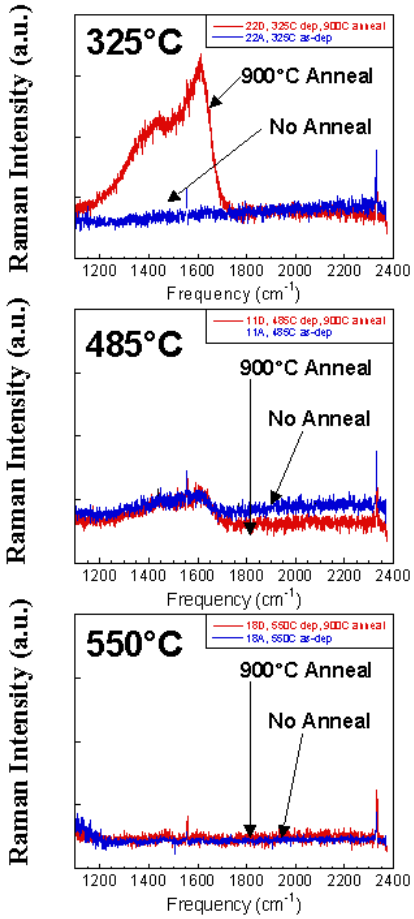

Figure 3.10: Raman spectroscopy for TDEAH HfO_2 films deposited at 325 ºC, 485 ºC, and 550 ºC.

Based on the AES, SIMS, and Raman data used to analyze the impurity concentrations in the TDEAH films, the deposition temperature is the primary factor influencing the amount of precursor impurities incorporated into the film microstructure. Annealing has minimal impact on reducing the in-film impurities. Post-annealing causes an out-diffusion of silicon from the substrate into the film for the 550 ºC films annealed at 900 ºC, and influences the local bonding arrangement of carbon impurities in the as-deposited versus annealed films deposited at 325 ºC.

Spectroscopic Ellipsometry Analysis

The differences in crystal structure, and the effects of annealing HfO_2 films deposited using TDEAH, manifest in the spectroscopic ellipsometry data, in terms of the sharpness of the band edge related feature at 5.8 eV. However, the energy position of the band edge feature and the onset of strong absorption do not appear to be related to the deposition or annealing conditions.

At 550 ºC, plots of the imaginary dielectric constant (ε_2) vs. photon energy (eV), show the onset of strong absorption, and a sharp band edge related feature at 5.8 eV (Fig. 3.11). The sharpness of the band edge related feature increases with annealing temperature, and is likely due to an improvement in crystal quality and an increase in film density.

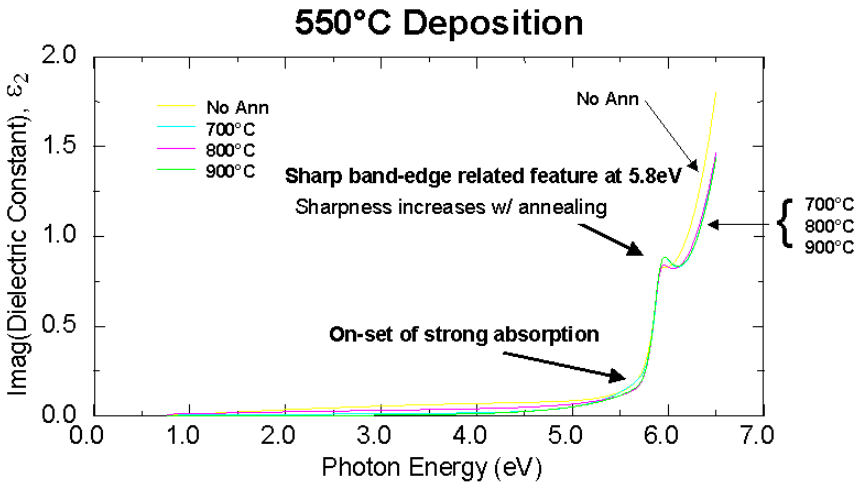

Figure 3.11: Spectroscopic ellipsometry at 550 ºC deposition temperature and various anneal conditions

At 485 ºC, the as deposited sample does not have the sharp band edge related feature at 5.8 eV. Notice the flat structureless character of ε_2 for the as deposited sample (Fig. 3.12). Diffraction data indicated that the as deposited sample was a mixture of tetragonal and monoclinic phases. Upon annealing, the band edge related feature becomes progressively sharper. The band edge related feature at 5.8 eV appears strongly related to the monoclinic polymorph of HfO_2.

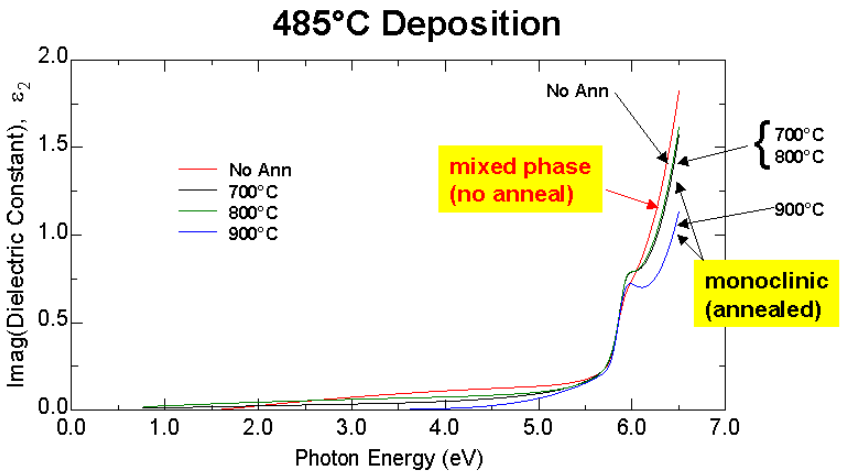

Figure 3.12: Spectroscopic ellipsometry at 485 ºC deposition temperature and various anneal conditions

Finally, for the 325 ºC deposition condition (Fig. 3.13), there is no clearly identifiable bandgap structure for any of the annealed conditions. However, a more defined absorption edge corresponding to the difference between the amorphous, as deposited film, and the tetragonal, annealed films is shown to exist.

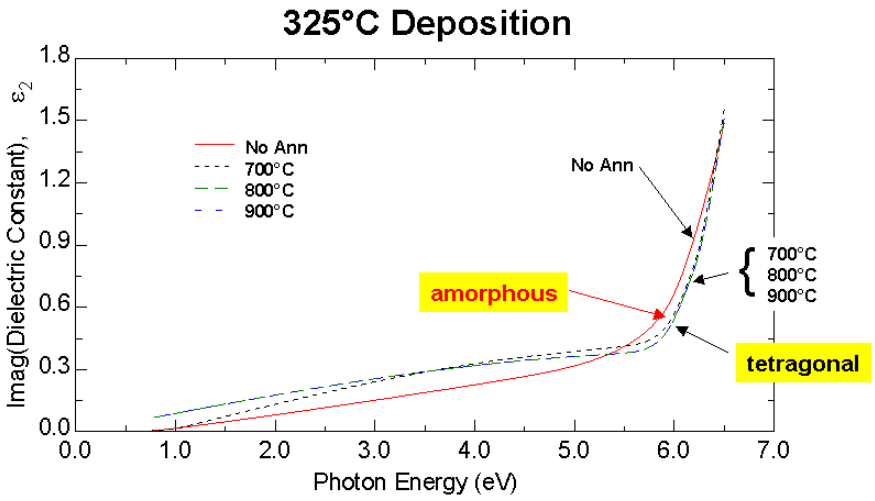

Figure 3.13: Spectroscopic ellipsometry at 325 ºC deposition temperature and various anneal conditions

The conclusion from the optical data is that the identifiable band edge related feature at 5.8 eV manifests for the monoclinic and not the tetragonal or amorphous samples. The presence of this band edge related feature indicates a difference in band structure between the monoclinic and tetragonal or amorphous phases of the HfO_2 films. To gain further insight it is prudent to look at some of the other investigations of the electronic structure of HfO_2 which have been performed using X-ray absorption spectroscopy (XAS),[153,154,155] spectroscopic ellipsometry,[156,157] and calculations.[158] These studies indicate that the valence band is comprised of O 2p states and that the conduction band is derived from Hf 5d states. XAS studies clearly reveal a crystal field splitting of the Hf 5d states. The crystal field splitting of the Hf 5d states will differ between the high-symmetry tetragonal phase and the lower-symmetry monoclinic phase of HfO_2. This difference in the crystal field splitting of the Hf 5d states is the probable origin of the band edge related feature observed in the spectra for the monoclinic samples.

The sharpness of the band edge related feature also increases with annealing temperature. This is likely related to improvements in the film density and crystal quality, as shown in the XRR data. The transition from the non-crystalline HfO_2 to the tetragonal HfO_2 resulted in a more defined absorption edge. This is to be expected since the amorphous HfO_2 has variations in bond angles and bond lengths that will blur the energy states that comprise the conduction band edge. Alternatively, the periodicity of crystalline HfO_2 results in a well defined absorption edge.

Density

An evaluation of HfO_2 films by XRR explains some of the density, and correspondingly, crystal quality improvements that manifest in the sharpness of absorption and band-edge features in the spectroscopic ellipsometry analysis. Plots of

density versus deposition temperature show an asymptotic like approach to the theoretical density of HfO_2 with increasing deposition temperature in the range of 325 ºC - 550 ºC. (Fig. 3.14) Subsequent post-annealing increases the film density more for the lower temperature depositions. For the films deposited at the higher deposition temperatures, the film density already approaches the theoretical density of 9.68 g/cm^3 for bulk HfO_2[159] as deposited, and post-annealing has a minimal effect on additional density increases.

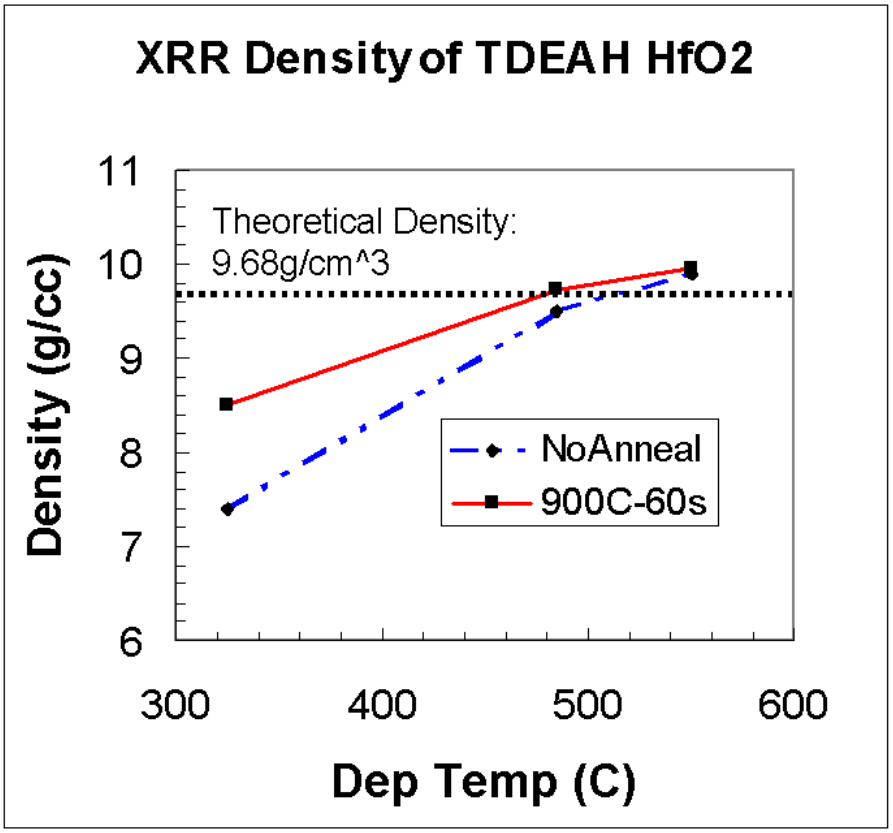

Figure 3.14: Density as a function of deposition temperature for as-deposited and annealed (900 ºC-60s-N_2) films

3.5 ELECTRICAL CHARACTERIZATION RESULTS AND DISCUSSION

Shadow-masked platinum gated MOS capacitors were fabricated to evaluate the electrical characteristics of TDEAH HfO_2 films. Capacitance vs. Voltage (C-V) and Current Density vs. Voltage (J-V) curves were performed on a thickness series of 30 Å, 50 Å, and 70 Å HfO_2 samples. In addition, C-V and J-V data were collected on the thinnest samples (30 Å) from the following anneal conditions; no anneal, 700 ºC - 60sec, 800 ºC - 60sec, and 900 ºC - 60sec. All substrates are n-type with a resistivity of 10 ohm-cm. Depositions at 550 ºC achieve a dramatic improvement in the electrical leakage properties compared to the 325 ºC and 485 ºC films. The leakage properties are strongly related to deposition and anneal temperature, and therefore, the carbon impurities, density, and possibly the band-edge differences are responsible for the drastic differences in electrical characteristics.

A comparison of C-V plots for 325 ºC, 485 ºC, and 550 ºC films annealed at 800 ºC - 60sec reveal distinct differences based on the deposition conditions. C-V plots for all deposition temperatures reveal a significant tail in accumulation for the films deposited at 325 ºC. This tail is typically associated with leakier samples when the C-V measurement is performed in series mode. The increased leakages for the 325 ºC films are also seen in the plots of current density vs. voltage.

An examination of the 485 ºC and 550 ºC plots indicates a similar, but less pronounced, tail for the thinnest (30 Å) samples deposited at 485 ºC. (Fig. 3.15) The samples deposited at 550 ºC do not exhibit any sort of tailing phenomena in accumulation. The best electrical results achieved in this matrix are for the 30 Å films deposited at 550 ºC. These films achieved a capacitance equivalent thickness of 14.4 Å and 0.05 Å /cm2 at V_{fb} + 1V (or 2.5V).

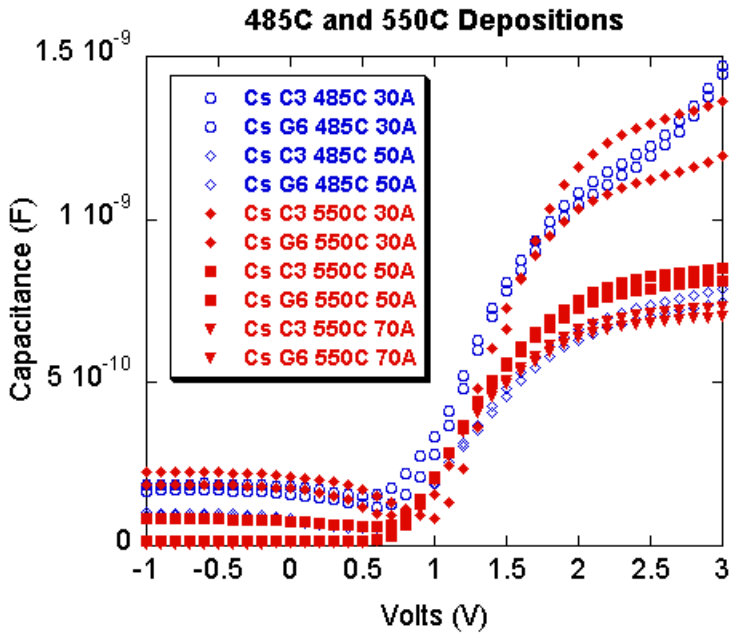

Figure 3.15: C-V plot for 485 ºC and 550 ºC deposition temperatures. The 485 °C samples show a slight C-V tail. All samples were annealed at 800 ºC for 60 sec

An analysis of the current density versus bias voltage reveals the differences in leakage as a function of film thickness and deposition temperature. (Fig. 3.16) All the films deposited at 325 ºC, regardless of film thickness, have identical J vs. V characteristics. This indicates the leakage characteristics are dominated by physical defects, not intrinsic film properties. The 485 ºC films show improved leakage properties. Unlike the 325 ºC films, the leakage of the 485 ºC films is dependent on the film thickness. An additional increase in deposition temperature to 550 ºC continues to improve the leakage characteristics. The leakage dependence on film thickness is even greater for the 550 ºC deposition condition than for the 485 ºC samples.

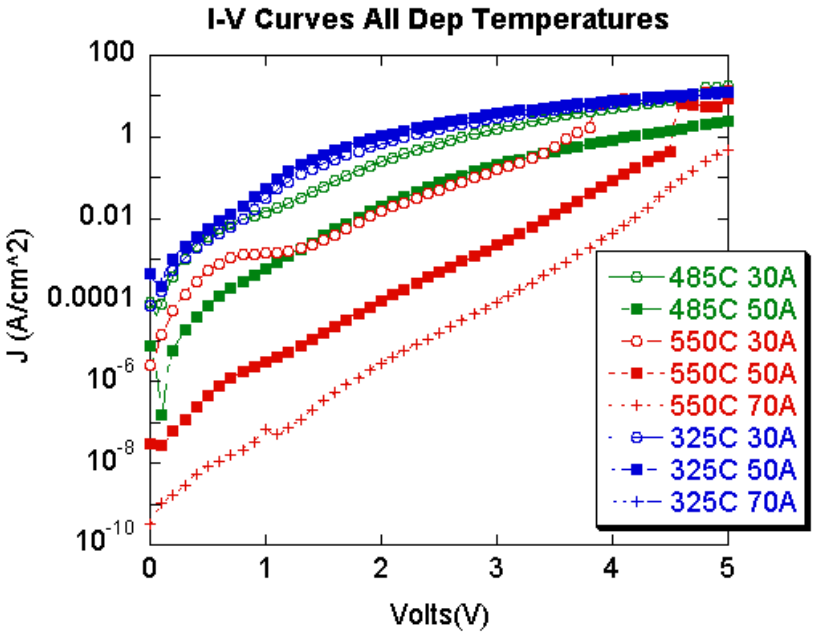

Figure 3.16: J vs. V plot for all deposition temperatures. The leakage properties of the 325°C are independent of film thickness; possibly due to the high C and N impurity distributions. All samples were annealed at 800 °C for 60 sec

3.6 CORRELATION OF ELECTRICAL AND PHYSICAL RESULTS

Increased deposition temperature dramatically improves the C-V and electrical characteristics of HfO_2 films. Extensive physical characterization has shown that the improvements in electrical leakage with deposition temperature are most likely due to reduced carbon impurity concentration or improved density of the HfO_2 films. Plots of leakage current vs. HfO_2 physical thickness show dramatic slope changes based on deposition temperature (Fig. 3.17). The 325 ºC films have a leakage behavior that is independent of HfO_2 physical thickness. The slope for the 485 ºC and 550 ºC films become progressively steeper with increased deposition temperature.

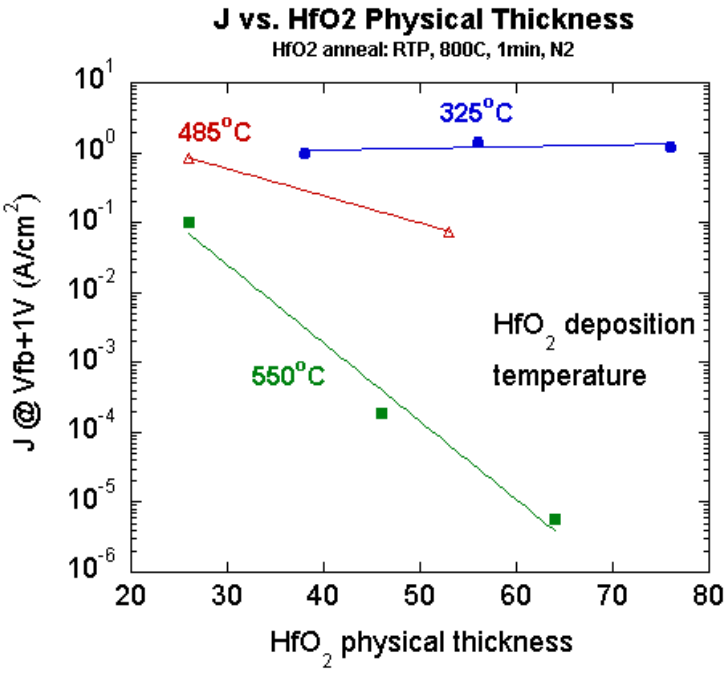

Figure 3.17: Plot of leakage current vs. HfO_2 physical thickness

Unfortunately, it is difficult to discern whether carbon impurities or HfO_2 density result in the leakage improvements because the density and carbon content are themselves interrelated. A plot of leakage current versus atomic percent carbon and HfO_2 density shows that by increasing deposition temperature from 325 ºC to 485 ºC, a large reduction in carbon impurities and a large increase in HfO_2 density is achieved. (Fig. 3.18) These improvements in film quality have a relatively minimal effect on the leakage characteristics. An additional increase in deposition temperature from 485 ºC to 550 ºC results in only minor reductions in carbon impurity levels and only small increases in HfO_2 film density. However, an apparent threshold exists between between 485 ºC and 550 ºC deposition temperatures because only slight reductions in impurity levels and small increases in film density result in large improvements to the gate leakage. The dramatic difference in leakage properties between 485 ºC and 550 ºC deposition temperatures may be related to the presence of carbon clusters within the HfO_2 films. The Raman analysis indicated the presence of sp^2 and sp^3 bound carbon clusters in all films except for the 550 ºC deposition conditions and the 325 ºC as-deposited condition. The 325 ºC as-deposited condition did not have a Raman peak because the film was amorphous and the carbon did not exist in cluster form until after annealing. At 550 ºC, SIMS analysis indicated lower absolute levels of carbon impurities, with no indication of cluster formation from the Raman spectroscopy data. The difference in carbon clusters between the 485 ºC and 550 ºC deposition conditions correlate with the large improvements in electrical leakage properties.

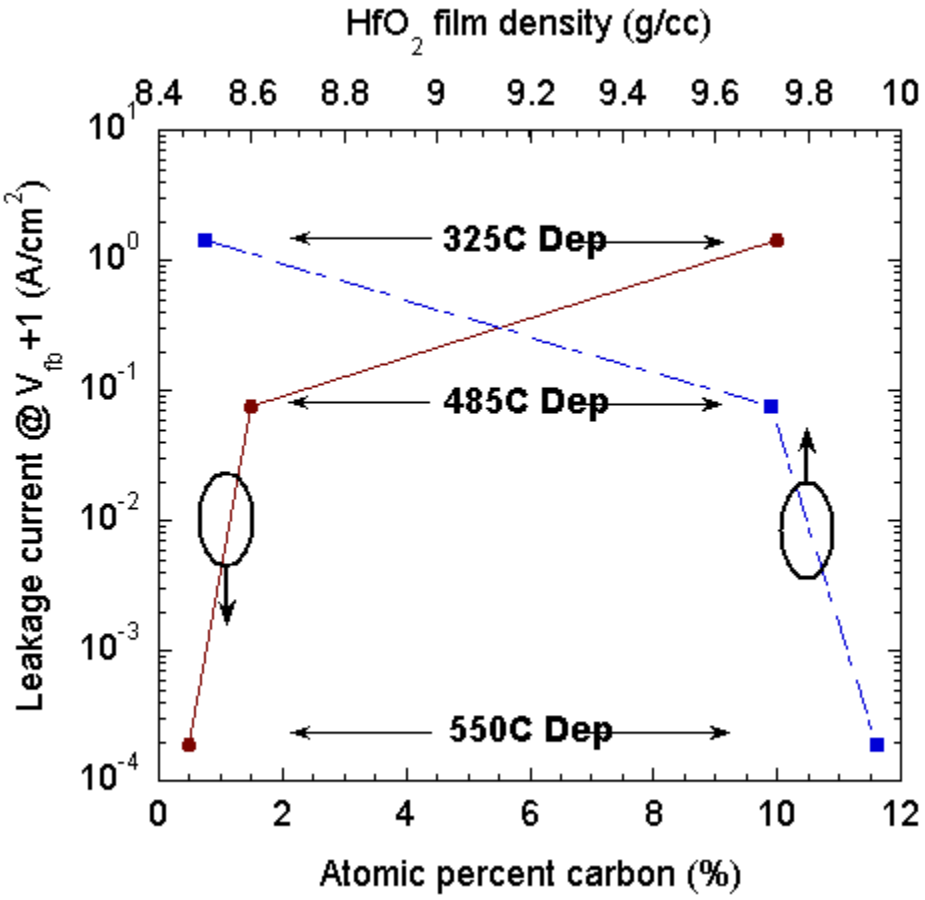

Figure 3.18: Leakage current as a function of atomic percent carbon and HfO_2 density

3.7 CONCLUSIONS

HfO_2 films grown using TDEAH precursor were evaluated as candidate high permittivity gate dielectrics. Deposition rates, film microstructure, impurity content, grain diameter, and density are highly dependent on the growth temperature. Increasing the deposition temperature enhances the leakage properties of HfO_2 gate dielectrics. These improvements are likely due to reduced carbon impurity content and higher density films achieved at the 550 ºC deposition temperature. The carbon impurities exist as clusters that degrade the electrical properties. It appears that when the carbon cluster density or size is reduced past a maximum threshold, dramatic improvements in the electrical characteristics are achieved.

Chapter 4: Physical and Electrical Properties of Metal Gate Electrodes Deposited on HfO_2 Gate Dielectrics

4.1 ABSTRACT

As the MOSFET gate lengths scale down to 50 nm and below, the expected increase in gate leakage will be countered by the use of a high dielectric constant (high-κ) gate oxide. The series capacitance from polysilicon gate electrode depletion significantly reduces the gate capacitance as the dielectric thickness is scaled to 10 Å equivalent oxide thickness (EOT) or below. Metal gates promise to solve this problem and address other gate stack scaling concerns like boron penetration and elevated gate resistance. Extensive simulations have shown that the optimal gate work-functions for the sub-50 nm channel lengths should be 0.2 eV below (above) the conduction (valence) band edge of silicon for n-MOSFETs (p-MOSFETs). This study summarizes the evaluations of TiN, Ta-Si-N, Ti-Al-N, WN, TaN, TaSi, Ir and IrO_2 as candidate metals for dual-metal gate CMOS using HfO_2 as the gate dielectric. The gate work-function was determined by fabricating MOS capacitors with varying dielectric thicknesses and different post-gate anneals. The metal-dielectric compatibility was studied by annealing the gate stacks at different temperatures. The gate stacks were characterized using TEM, SIMS, RBS, AFM, and XRD. Based on work-functions and thermal stability, Ta-Si-N and TaN show the most promise as metal electrodes for HfO_2 n-MOSFETs.

4.2 INTRODUCTION

In sub-50nm gate length MOSFETs, the parasitic series capacitance due to depletion in polycrystalline silicon (poly-Si) gates results in unacceptable reduction in the

gate capacitance and drive current. Metal gates have been studied for several years as replacements for poly-Si gates to address this problem. Advantages of using metal gate electrodes include a reduction of the gate resistance to counter the scaled gate heights, and elimination of boron penetration from the doped poly-silicon into the gate dielectric. Simulations of p and n MOSFETs with 40-50 nm gate lengths indicate that the optimal gate work-functions to maximize drive current are ~0.2eV away from the valence band (ϕ_m = 5.0-5.2 eV, PMOS) and conduction band (ϕ_m =4.1-4.3 eV, NMOS) edges.[160,161]

It has previously been documented that compatibility issues between ZrO_2 and HfO_2 dielectrics with poly-silicon electrodes exist.[162] The large radius and electronegativity differences between metal and silicon atoms result in undesirable silicide reactions upon annealing. In the case of metal oxide – metal gate systems, due to the similarities in the electronegativity and radii of metals employed, gate stack inter-diffusion is commonly observed. Mutual solubility, which enables inter-diffusion, depends on similarities in crystalline structure, atomic electronegativity, and atomic size.[163]

One possible mechanism of gate stack inter-diffusion is for the electrode material to diffuse into the gate dielectric. This most likely occurs by means of short-circuit diffusion, or diffusion through the grain boundaries of the poly-crystalline oxide.[164] Another potential mechanism for gate stack inter-diffusion has been reported where Zr from ZrO_2 was shown to be dissolved into Pt at low oxygen partial pressures.[165] One would expect for the gate stack integrity to be compromised once the primary cation species from the metal oxide dielectric begins dissolving into the metal electrode.

However, depending on the metal gates evaluated, some interfacial reactions are also possible. If reactions or inter-diffusions do occur, a shift in the device properties with annealing conditions such as *CET* (Capacitance Equivalent Thickness), V_t

(Threshold Voltage), or I_g (Gate Leakage) may be observed. Various metal gate / HfO_2 interfaces have been evaluated to detect possible interfacial reactions. In addition, significant grain growth, or microstructure changes at source/drain annealing temperatures may roughen the gate/dielectric interface, or change the work function of the metal gate. Instabilities like these can impact device characteristics such as mobility or V_t. Finally, the deposition technique itself may induce fixed charges in the gate dielectric and should be considered in the metal gate selection process.

A wide variety of metal gates are currently being evaluated as replacements for n+ and p+ poly on high permittivity gate dielectrics in CMOS circuits at the 50 nm node. Understanding the metal gate electrode - gate dielectric interface is critical to understanding device performance. In this study, the physical properties of eight metal gate electrodes have been characterized in contact with HfO_2 gate dielectric, a promising high permittivity gate dielectric candidate. These materials and interface studies elucidate which classes of metal gates are promising NMOS and PMOS electrode candidates.

4.3 EXPERIMENT

The HfO_2 gate dielectric was deposited by metal organic chemical vapor deposition (MOCVD) at 550°C with Hf tert-butoxide precursor [Hf-$(OC_4H_9)_4$]. The dielectric was poly-crystalline as deposited. All metals investigated in this study were deposited via PVD (physical vapor deposition). Metal/HfO_2 stacks annealed at different temperatures in an inert Ar ambient were used for physical characterization. Most stacks were characterized using SIMS, TEM, and XRD. Some of the stacks were also analyzed using RBS and AFM.

For work-function evaluation, metal-oxide-semiconductor capacitors (MOSCAPs) on either N or P-type Si substrates were fabricated. The metal electrodes were capped with W to provide a low resistance contact and the gates were patterned using plasma etching of the metal stacks. Subsequently, some devices were subjected to different post-gate anneals of 900°C/60s or 1025°C/10s in an inert ambient. All capacitors were subjected to either a 390°C or 450°C (H_2+N_2) forming gas (FG) anneal for 30 min. MOSCAPs with an area of 1×10^{-4} cm^2 were used for *C-V* (Capacitance vs. Gate Voltage) and I_g-V_g (Gate Current vs. Gate Voltage) characterization. The work-function was determined from plots of flat-band voltage (V_{fb}) versus capacitance equivalent thickness (*CET*). Since $V_{fb} = \phi_{ms} - Q_i*CET/\varepsilon_{SiO2}$, where Q_i is the effective oxide charge at the oxide interface and ε_{SiO2} is the SiO_2 permittivity, the slope in the V_{fb} vs. *CET* plot gives the magnitude and sign of the oxide fixed charge and the intercept provides the work function potential difference, ϕ_{ms}. From ϕ_{ms}, and the equation, $\phi_{ms} = \phi_m - \phi_s$, the metal work function, ϕ_m, can be calculated. The Fermi energy of silicon, ϕ_s, is equal to ϕ_s=4.61+$kT\ln(N_a/n_i)$ for p-substrates and ϕ_s=4.61-$kT\ln(N_d/n_i)$ for n-substrates, where N_a, N_d, and n_i are the acceptor, donor, and intrinsic carrier concentrations, respectively. The quantity 4.61 eV is the energy required to remove an electron from intrinsic silicon to vacuum.

4.4 RESULTS

Tantalum-Silicon-Nitride (Ta-Si-N) Electrodes

Tantalum-silicon-nitride has been reported as a useful NMOS metal,[166.167,168] e-beam lithography mask,[169] and diffusion barrier.[170] Ta-Si-N was formed by reactively sputtering a $Ta_{0.7}Si_{0.3}$ target in a N_2 ambient. Films with 20-40 atomic % N were

characterized for thermal and chemical stability. The deposition process results in a metastable amorphous microstructure of Ta-Si-N. X-ray diffraction analysis of sputtered Ta-Si-N films indicates that the amorphous microstructure is stable up to 1025°C (Fig. 4.1). A broad diffraction peak spanning 32°-42° 2θ for the Ta-Si-N films at all anneal conditions indicates that the microstructure is either very fine-grained or completely amorphous. No sharp peaks indicative of TaN_x or $TaSi_x$ phases are observed after annealing. Cross-section TEM and selected area diffraction also indicate that the Ta-Si-N microstructure is amorphous (Fig. 4.2). The benefit of the amorphous microstructure is that no grain boundaries are available for Hf out-diffusion from the metal oxide dielectric. In metal-silicon-nitride films, the metal and nitrogen and the silicon and nitride form a quasi-binary system. The stability of the amorphous phase is due to kinetic restraints that hinder crystalline nucleation. In TM-Si-N systems (TM = transition metal), the TM_1N_1 and Si_3N_4 differ drastically in their crystal structure and bonding. This leads to limited solubility of the two binary phases and a metastable amorphous structure.[171] The exceptional barrier properties of Ta-Si-N films are shown by SIMS depth profiling of a Ta-Si-N/HfO_2/Si gate stack. The metal gate dielectric interface is shown to be stable up to 1025°C (Fig. 4.3).

It was observed that the work-function of Ta-Si-N/SiO_2 is independent of N content in the 20-40 atomic % range. For this study, Ta-Si-N films with ~26% N were chosen as the gate electrode. Contrary to these results, another study on this subject observed shifts in the ϕ_m of Ta-Si-N with increasing N concentration.[172] For those studies, increasing the N concentration resulted in V_{fb} shifts that are indicative of a higher ϕ_m. This study also speculates that the presence of Si in Ta-Si-N suppresses N diffusion into the SiO_2 dielectric since N diffusion into the dielectric was observed for TaN electrodes, but not for Ta-Si-N electrodes. Figure 4.4 shows the work-function and the

capacitor equivalent thickness (*CET*) change with thermal budget for different Ta-containing electrodes evaluated in this study. TEM characterization indicates that the increase in *CET* is due to interfacial layer growth between HfO_2 and the Si substrate. The work-function variation with thermal budget is real and is observed with all electrodes investigated. This suggests that the work-function is modified by small composition and/or structural variations at the metal/crystalline dielectric interface. The Ta-Si-N work-function of ~4.4eV after a high temperature anneal makes it an attractive candidate for n-MOSFETs.

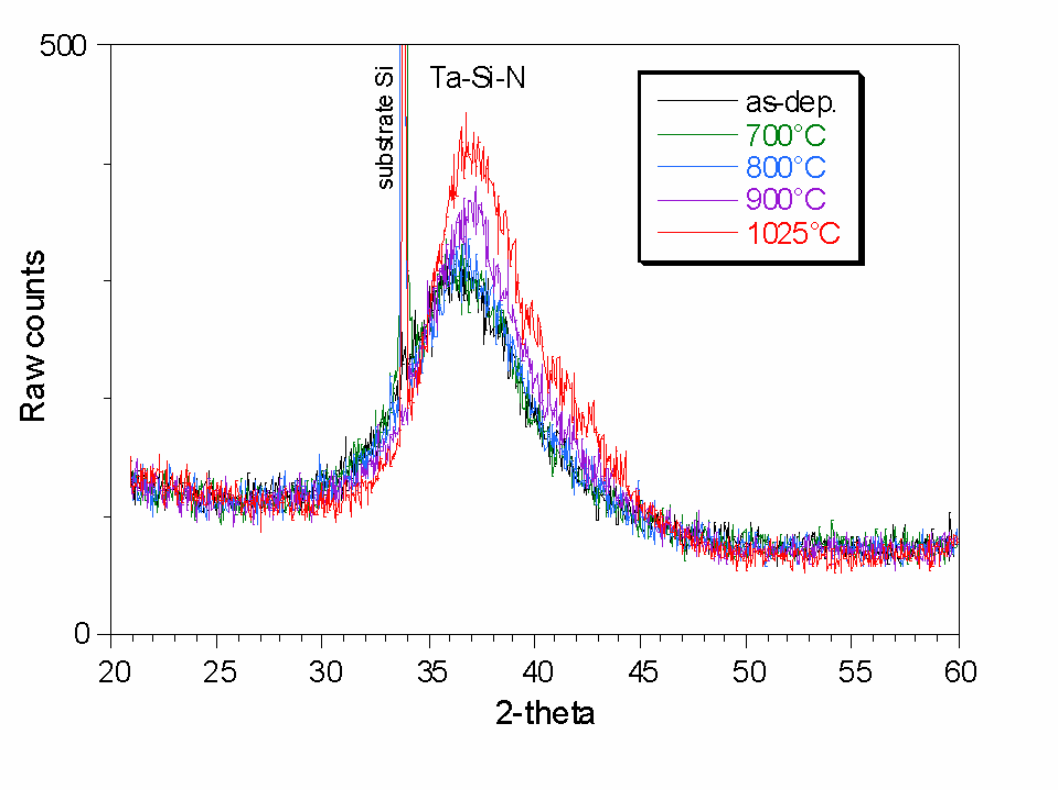

Figure 4.1: XRD for a Ta-Si-N gate electrode indicating a stable microstructure up to 1025°C. No sharp peaks indicative of TaSi or TaN phases appear upon annealing.

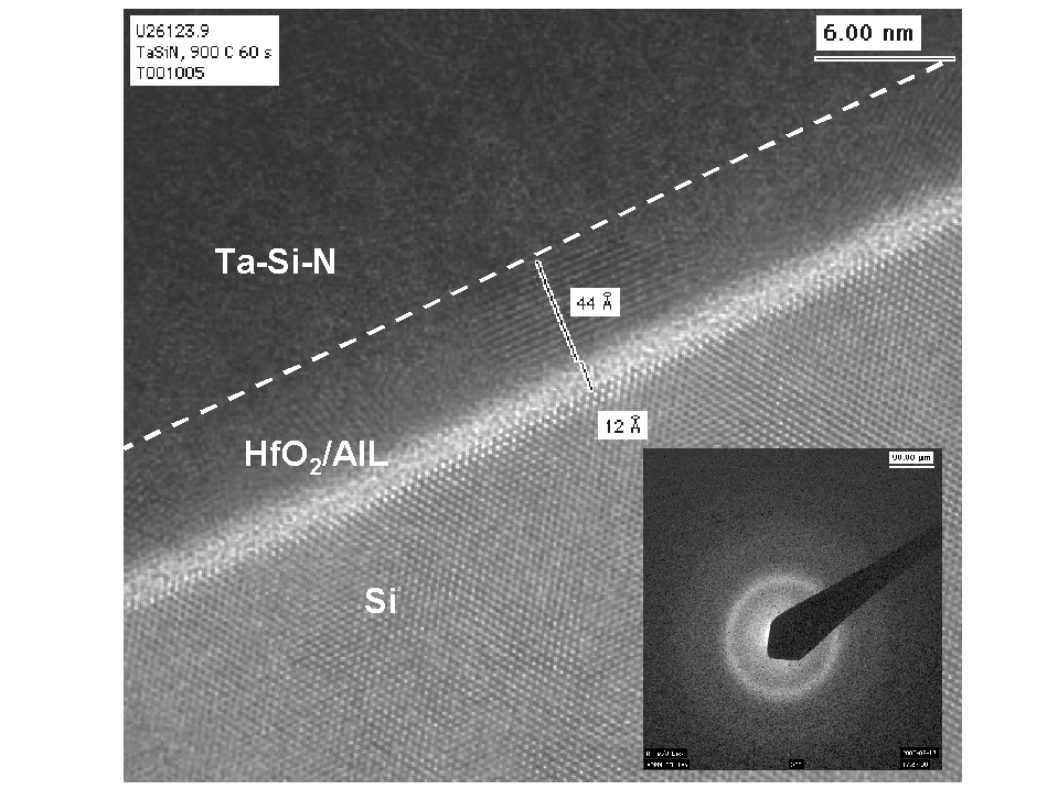

Figure 4.2: Bright field TEM and TED showing a stable Ta-Si-N / HfO_2 interface and metastable amorphous microstructure of Ta-Si-N.

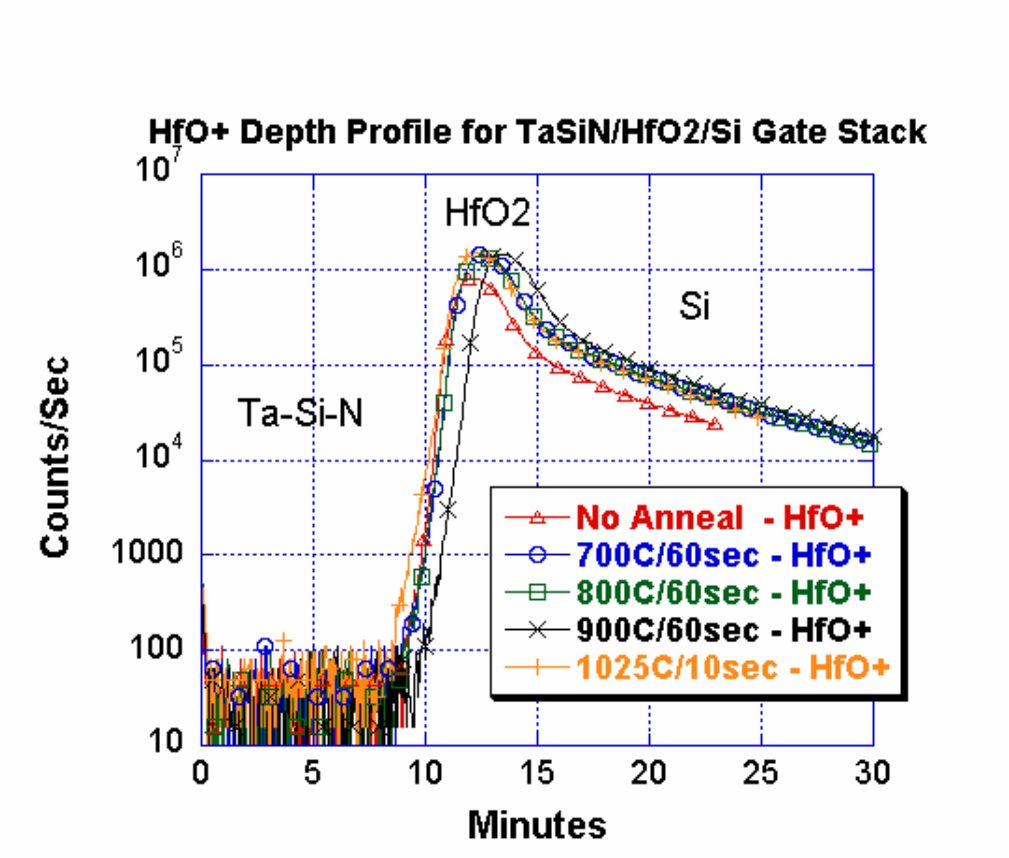

Figure 4.3: SIMS depth profile of HfO+ ion showing a stable Ta-Si-N / HfO_2 interface up to 1025°C.

Tantanlum Nitride (TaN) Electrodes Tantalum Silicide (TaSi) Electrodes

Tantalum nitride electrodes were formed by sputtering Ta in a N_2/Ar ambient. XRD analysis indicated prominent fcc-TaN (111) and (200) peaks. SIMS analysis of W/TaN/HfO_2 gate stacks annealed at different temperatures indicated no inter-diffusion or reactivity up to 900°C. There was some Hf and Ta inter-diffusion after a 1025°C anneal. Nitrogen in TaN is relatively stable upon annealing up to 1025°C. TEM analysis of the same stacks confirms that no reaction exists between TaN and HfO_2 at 900°C and 1025°C. The TEM analysis also indicates that the capacitance equivalent thickness increase (Fig. 4.4) is due to interfacial layer (IL) growth. TaN and Ta-Si-N have similar work-functions after the gate stack is annealed which suggests that TaN could also be a potential metal gate candidate for high-κ n-MOSFETs.

Tantalum Silicide (TaSi) Electrodes

The $TaSi_x$ films were sputtered from a $Ta_{0.7}Si_{0.3}$ target in an Ar ambient. SIMS analysis of W/$TaSi_x$/HfO_2 stacks indicates broadening of the $TaSi_x$/HfO_2 interfacial layer for temperatures >900°C suggesting $TaSi_x$ reaction with HfO_2. Also, for temperatures >900°C an increase in the SIMS oxygen intensity at the interface suggests a change in the matrix compared to the as deposited stack. The average CET increase after a 1025°C anneal is ~9Å which is higher compared to other metal gates at similar thermal budgets. $TaSi_x$ possesses a higher work-function compared to TaN or Ta-Si-N after annealing, making it less attractive for NMOS applications. The increase in CET with annealing for $TaSi_x$ may be due to increased reactivity between the gate dielectric and the electrode for non-nitride refractory electrode materials.

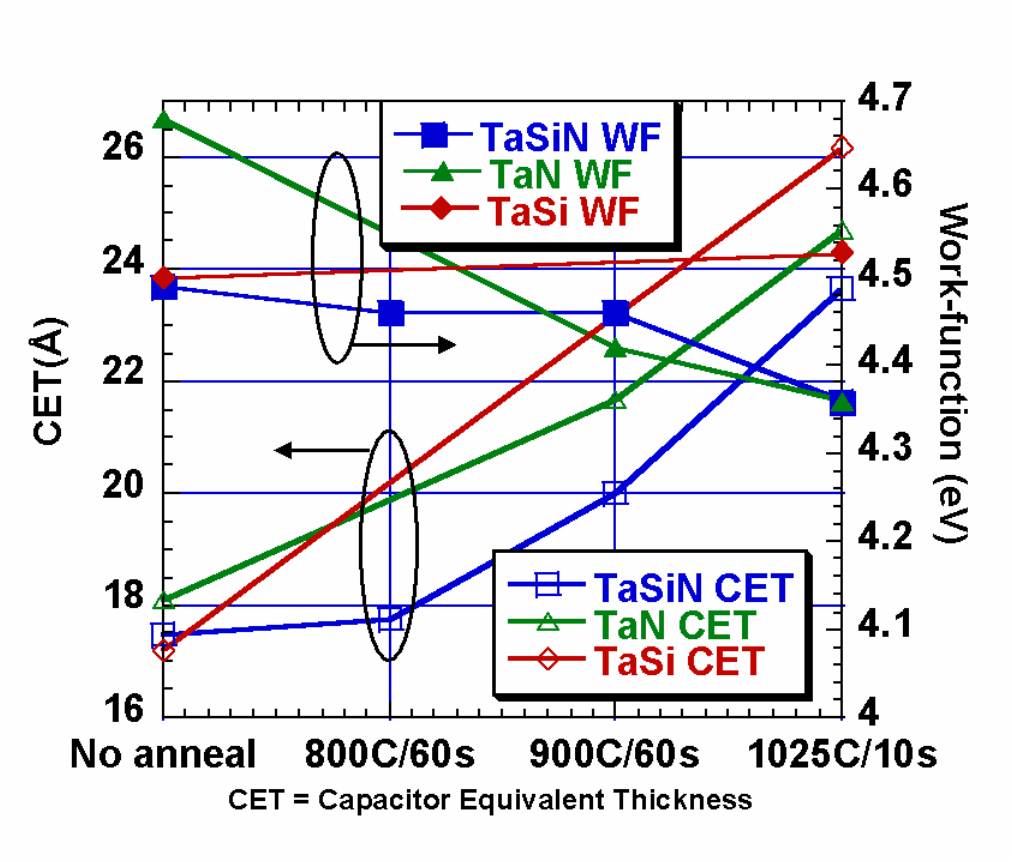

Figure 4.4: CET and work-function for different Ta-based metal gates/HfO_2 capacitors as a function of post-gate anneal temperature.

Tungsten Nitride (WN) Electrodes

Tungsten nitride films sputter deposited on HfO_2 dielectrics were also evaluated as a potential PMOS electrode candidate. RBS analysis indicates a W/N atomic % ratio of 60/40 and not 50/50 as expected. XRD of as-deposited films shows a broad low-intensity peak suggesting a fine-grained poly-crystalline mixture of W_2N and WN phase. Upon annealing the film, diffraction data indicates an increase in intensity of (111) and (200) W_2N and (110) W peaks (Fig. 4.5). SIMS analysis of the W_2N gate stack also reveals a reduction in nitrogen levels with increased annealing temperatures (Fig. 4.6). There is an approximate 20% reduction in nitrogen concentration for the 800°C and 900°C anneal conditions. At 1025°C, the nitrogen concentration is reduced by approximately 60%. SIMS analysis of the Hf and W depth profiles show no evidence of inter-diffusion. The roughness increases from 0.216 nm root-mean-square (RMS) as-deposited to 5.075 nm RMS after a 900°C-60s anneal, likely a result of the observed microstructure changes. In addition, TEM analysis shows substantial growth of the interfacial oxide layer between the HfO_2 and the Si for annealed films with a WN electrode (Fig. 4.7). The amount of interfacial layer growth is larger than that observed for other metal gate electrodes. The phase instability of WN_x at dopant activation anneal temperatures eliminates it as a metal gate electrode candidate. The behavior of N in WN is quite different compared to N in TiN, TaN or Ta-Si-N where the nitrogen content was found to be stable after high temperature anneals.

The capacitor CETs for WN gated electrodes increase with post-gate anneal temperature (+3 Å after 900°C and +6 Å after a 1025°C anneal). TEM characterization attributes the increase in *CET* to growth of the HfO_2/Si interfacial layer. The work-function of WN/HfO_2/n-sub was found to be 4.22 eV (no-anneal) and 4.35 eV (900°

C/60s). The V_{fb}-*CET* data after a 1025 °C anneal were too scattered to calculate the work-function with any certainty. Given the phase instability and low-measured work-function on n-sub capacitors, WN is not a candidate for PMOS metal gate electrodes.

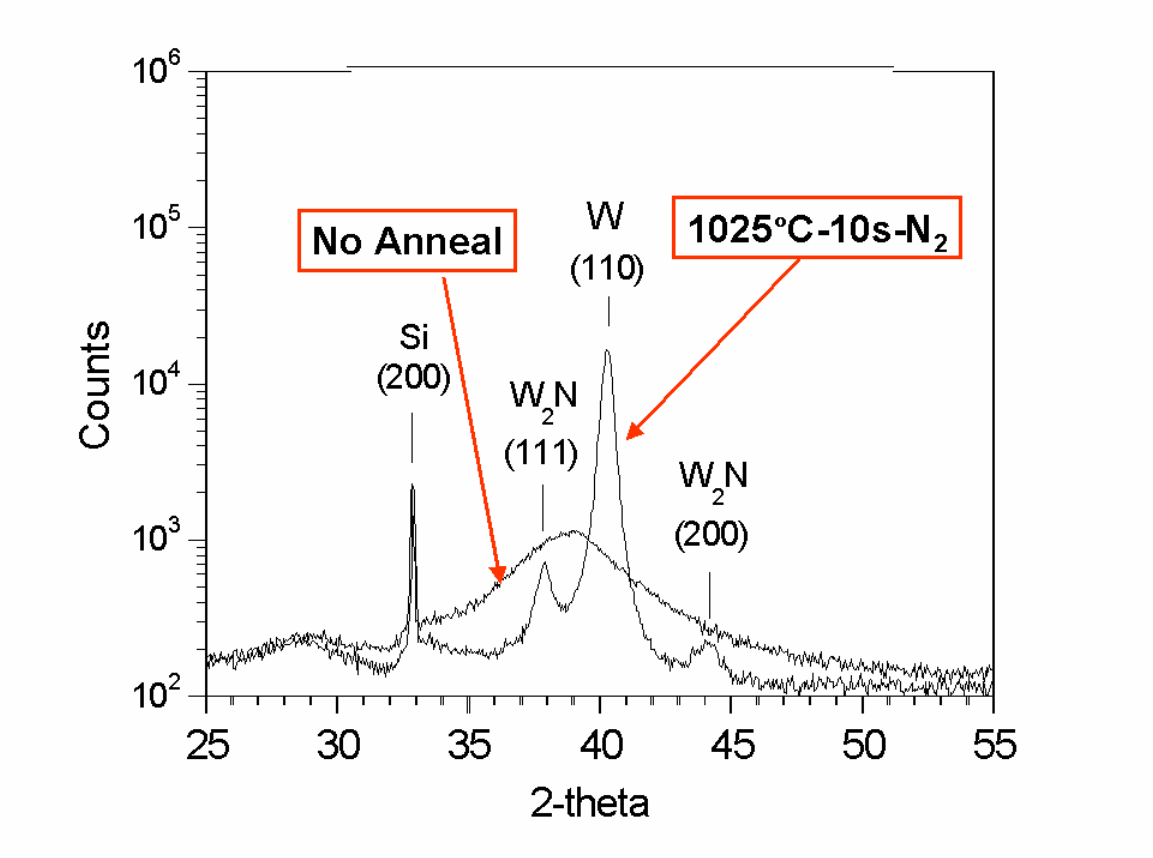

Figure 4.5: XRD of WN films as-deposited and after a 1025°C anneal.

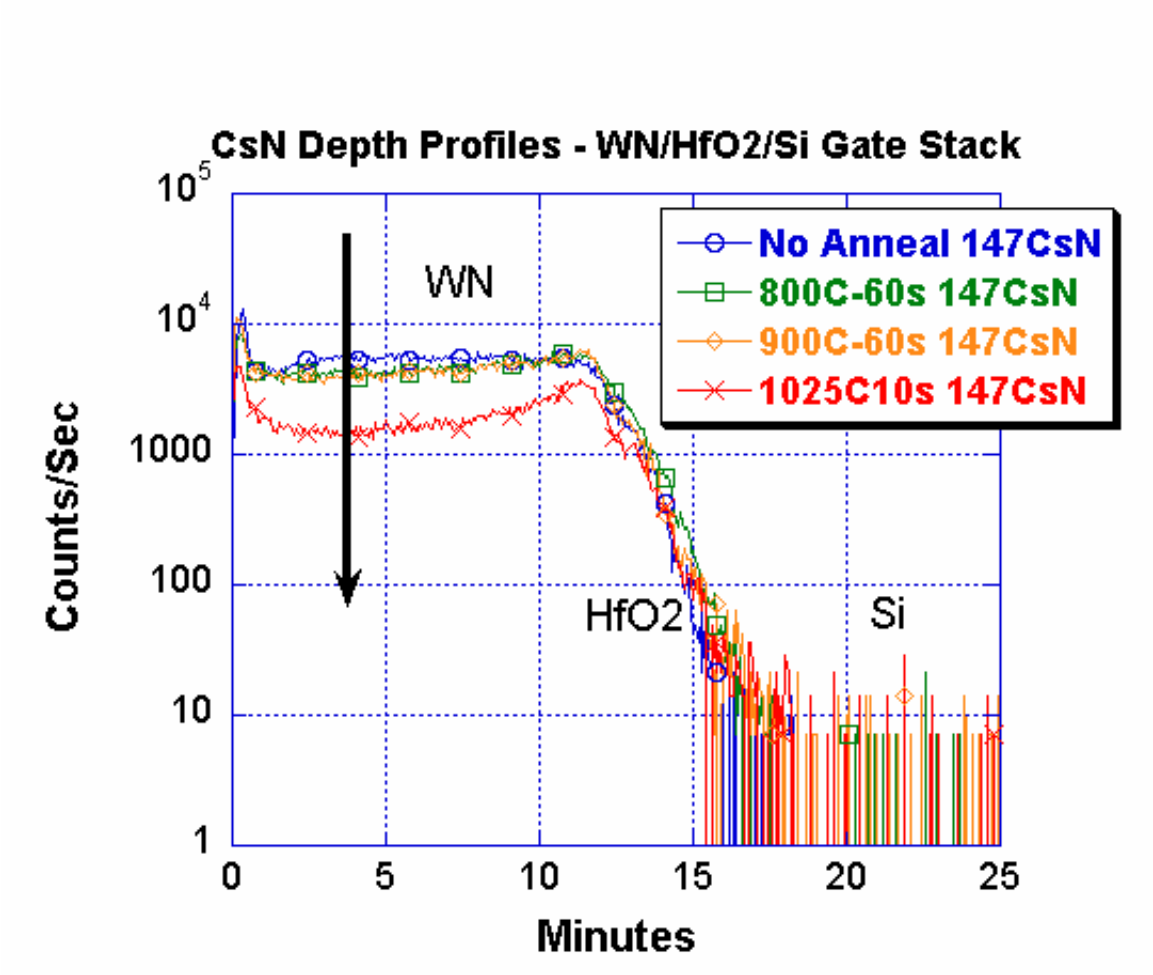

Figure 4.6: SIMS depth profile indicates a reduction in nitrogen with increasing anneal temperature for WN electrodes.

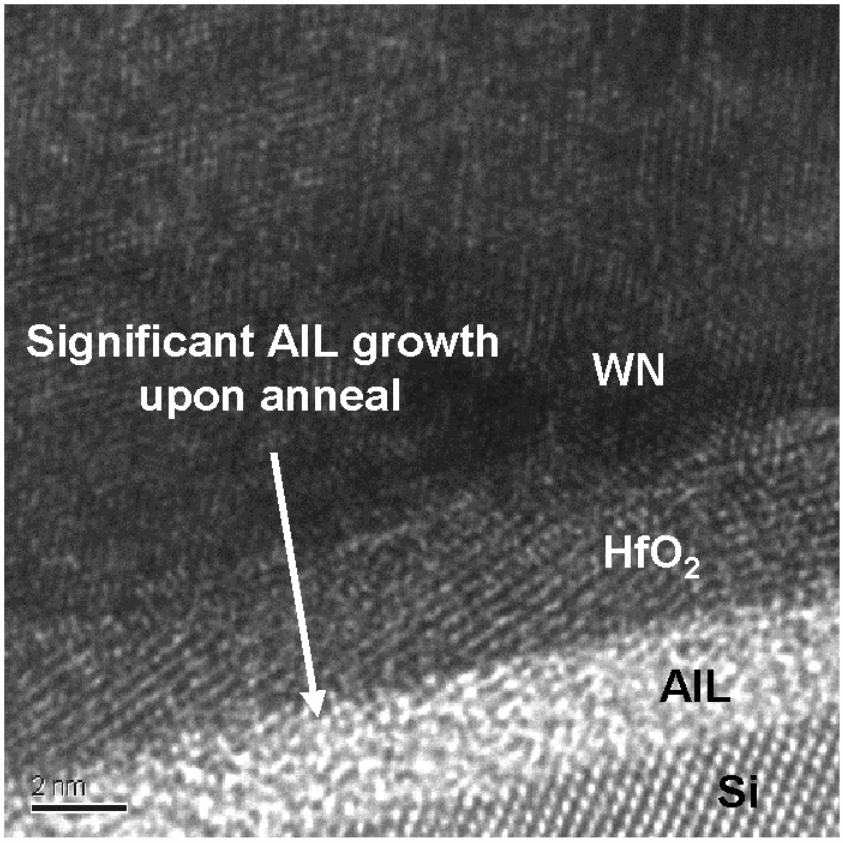

Figure 4.7: TEM reveals a stable WN / HfO_2 interface, but a significant amorphous interfacial layer (IL) growth is observed after annealing HfO_2 samples with a WN electrode.

Iridium (Ir) and Iridium Oxide (IrO_2) Electrodes

A sputter chamber with an iridium target was used for the deposition of iridium oxide and iridium gate electrodes for potential PMOS electrode applications. The IrO_2 films were deposited in an Ar/O_2 ambient. Sputter deposition of smooth IrO_2 films is difficult.[173] The film stress and roughness depend strongly on the substrate (SiO_2 vs. HfO_2) and deposition temperature. Annealing uncapped IrO_2 films results in a reduction of the IrO_2 film into faceted islands of iridium. XRD data shows the conversion of as-deposited IrO_2 films into iridium films at annealing temperatures of 800°C and 900°C in an N_2 ambient (Fig. 4.8). Thus, like WN_x films, the IrO_2 films do not exhibit sufficient phase stability at dopant activation annealing temperatures. Regardless, an attempt to cap the IrO_2 films with tungsten to prevent the loss of oxygen to the ambient during annealing was attempted for MOS capacitor evaluations. A transmission electron micrograph with energy dispersive spectroscopy (EDS) of a $W/IrO_2/HfO_2/Si$ gate stack after a 900°C anneal reveals that even with the tungsten cap layer the IrO_2 is completely reduced (Fig. 4.9). A thick WO_x layer forms between the tungsten and the original IrO_2 layer. A mixture of W and Ir is observed where the as-deposited IrO_2 was located. SIMS depth profiling also detected the presence of a thick WO_x layer (Fig. 4.10). EDS and SIMS data indicate the presence of Hf within both oxide layers after annealing, the WO_x layer and the original HfO_2 layer.

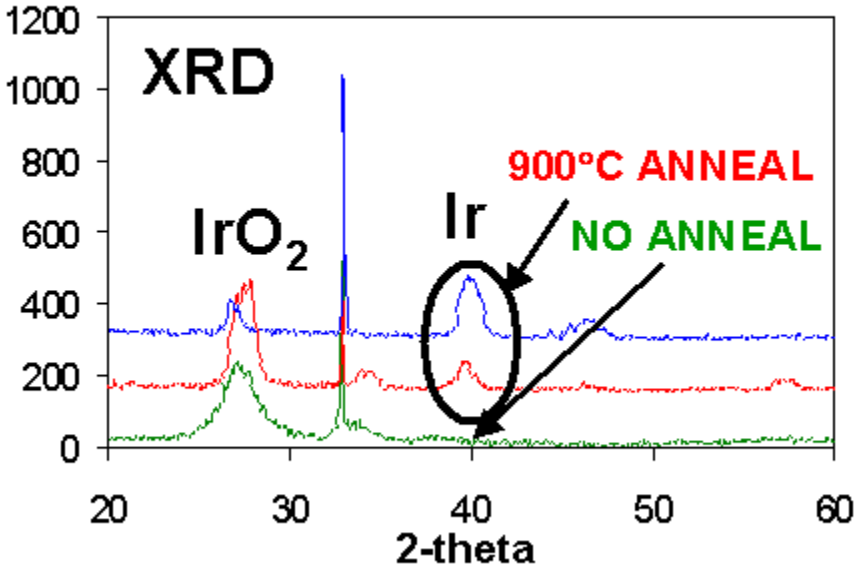

Figure 4.8: XRD showing a reduction of IrO_2 electrodes to a mixture of Ir and IrO_2 after a 900°C anneal.

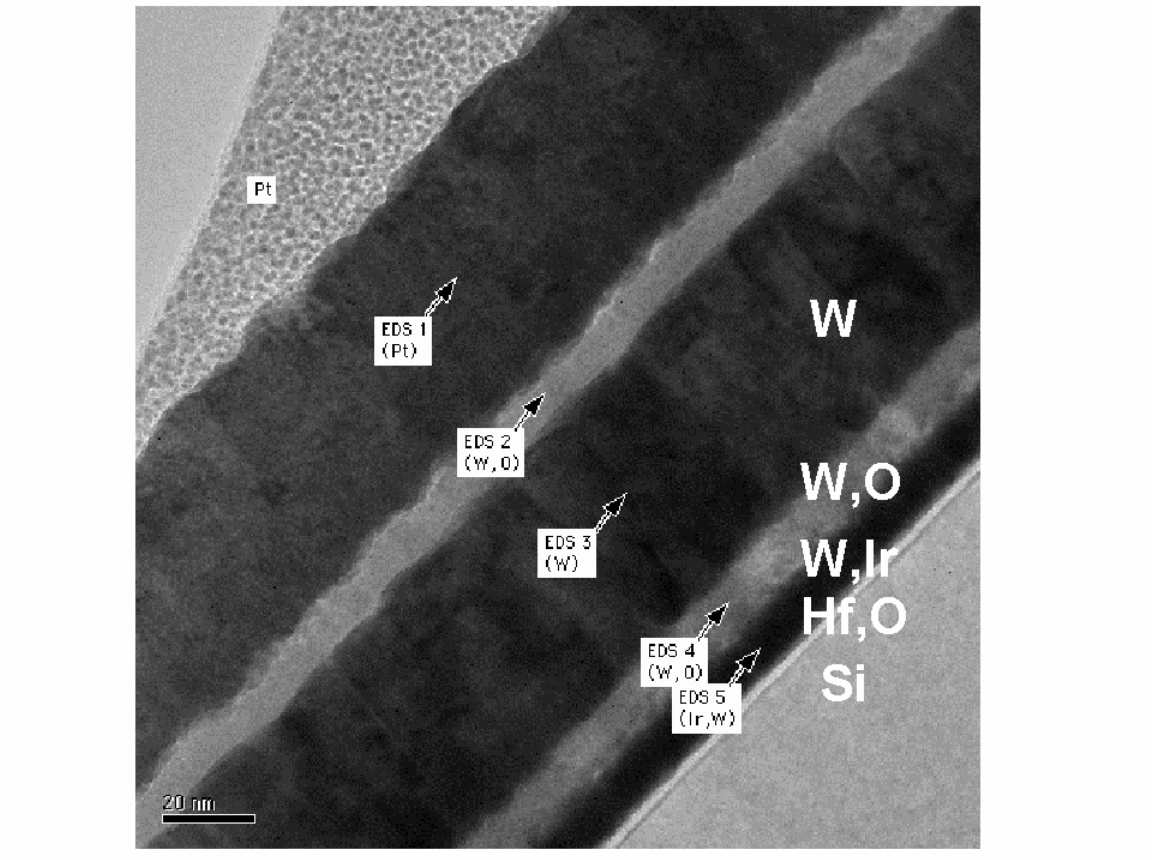

Figure 4.9: TEM of W/IrO_2/HfO_2 gate stack after a 900°C anneal showing the formation of a W and O containing interfacial layer between at the original W / IrO_2 interface.

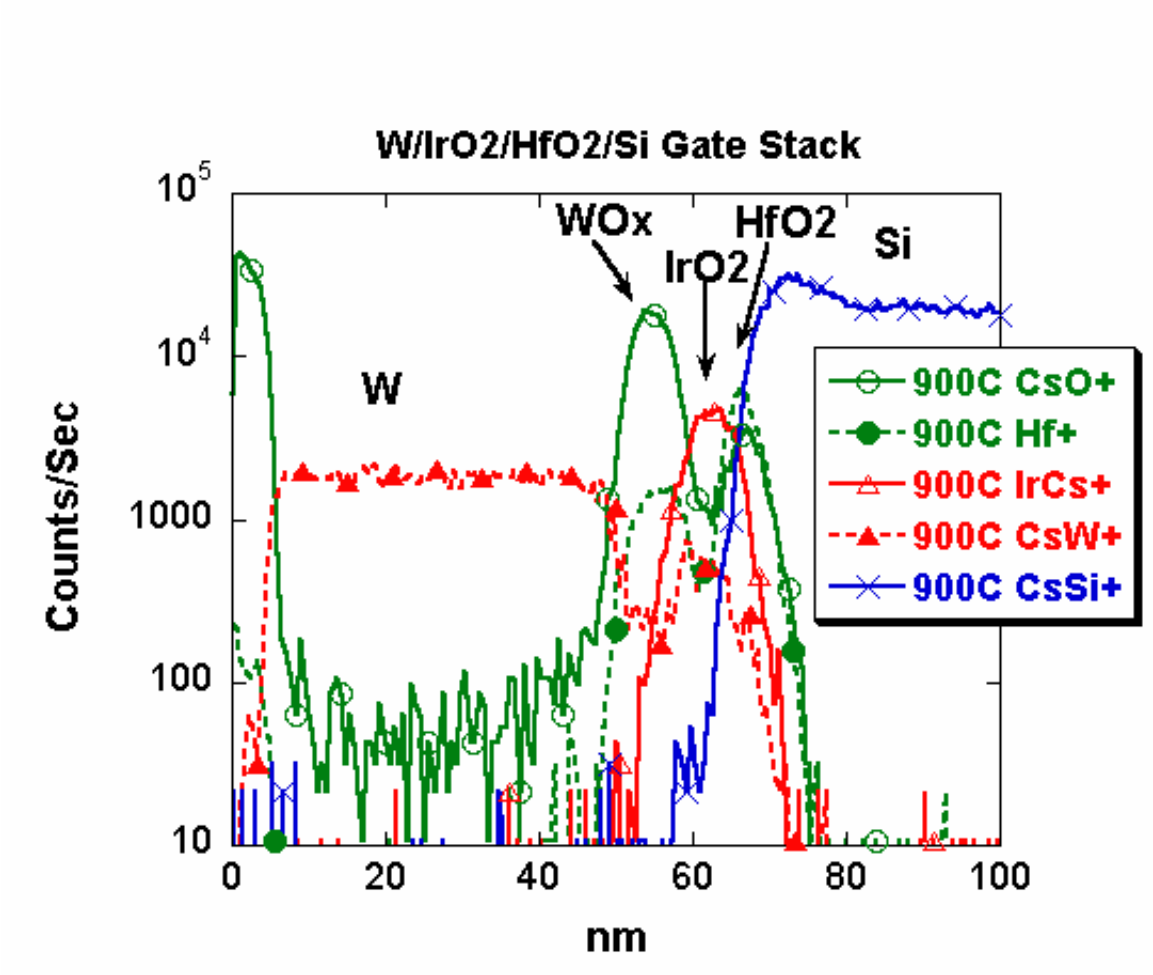

Figure 4.10: SIMS depth profile of $W/IrO_2/HfO_2$ gate stack showing the interfacial reactions between W and IrO_2.

Iridium electrodes were reactively sputtered in Ar ambient. Inter-diffusion, as opposed to interfacial reaction, is prevalent in the W/Ir/HfO2/Si gate stack. The inter-diffusion is easily noted with SIMS profiling (Fig. 4.11). Inward diffusion of tungsten into the iridium and HfO_2 is observed for anneals of 800°C and 900°C. Iridium from the electrode out-diffuses into the tungsten and diffuses inward towards the substrate. Hafnium from the HfO_2 film also out-diffuses into the iridium electrode. The hafnium

does not appear to diffuse into the silicon substrate. The SIMS "knock-on" effect is responsible for the Hf tail into the substrate. The tail appears similar to previously analyzed samples that are known to have no Hf diffusion into the substrate. There is also no observable difference in the hafnium depth profile in the substrate for the 800°C and 900°C annealing conditions that would indicate a thermally activated diffusion of hafnium into the silicon. Upon cleaving the annealed Ir/HfO_2 samples, the iridium films peeled off the substrate displaying adhesion problems with iridium electrodes. The use of elemental electrode candidates such as iridium, ruthenium, platinum, or possibly even alloyed candidates might not satisfy the gate stack thermal stability requirements due to excessive chemical diffusion.

Figure 4.12 shows the work-function and *CET* variation for Ir and IrO_2-electrode HfO_2 MOSCAPs. IrO_2 gates with only a forming gas anneal exhibit a work-function of 5.1 eV, which is ideal for p-MOSFETs. However, IrO_2 is easily reduced and the evolved oxygen causes the IL and CET to increase significantly. Iridium is chemically stable and does not cause the CET to increase as rapidly with increasing thermal budget. In addition, iridium tends to inter-diffuse easily and does not have as high a work-function on HfO_2 as expected. Based on this study it is felt that Ir and IrO_2 might not be suitable dual-metal candidates on HfO_2.

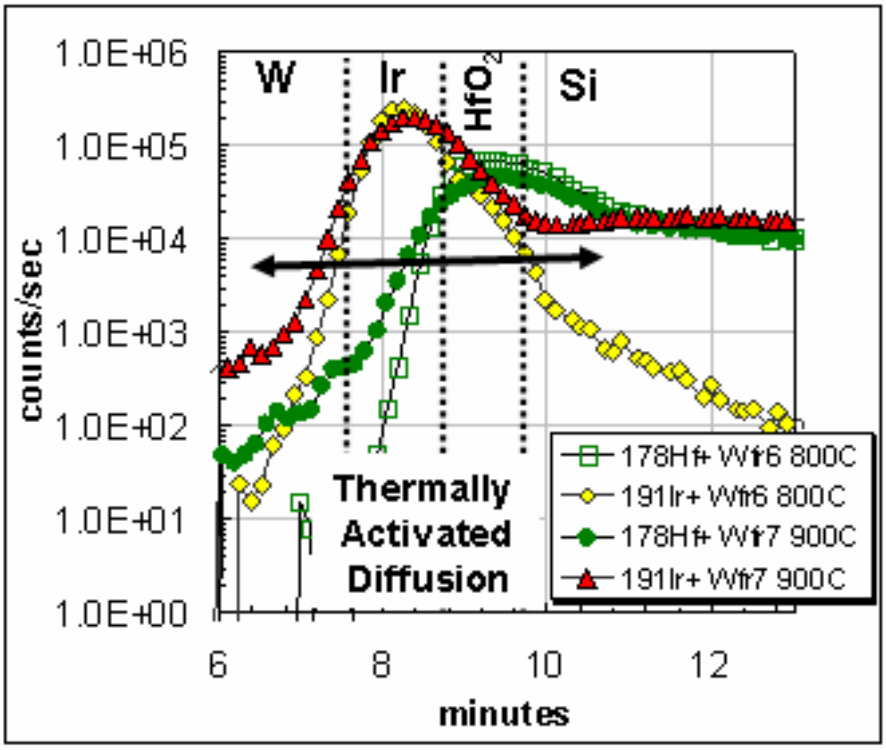

Figure 4.11: SIMS depth profile of W/Ir/HfO_2 gate stack showing inter-diffusion of Iridium into the W cap layer and HfO_2.

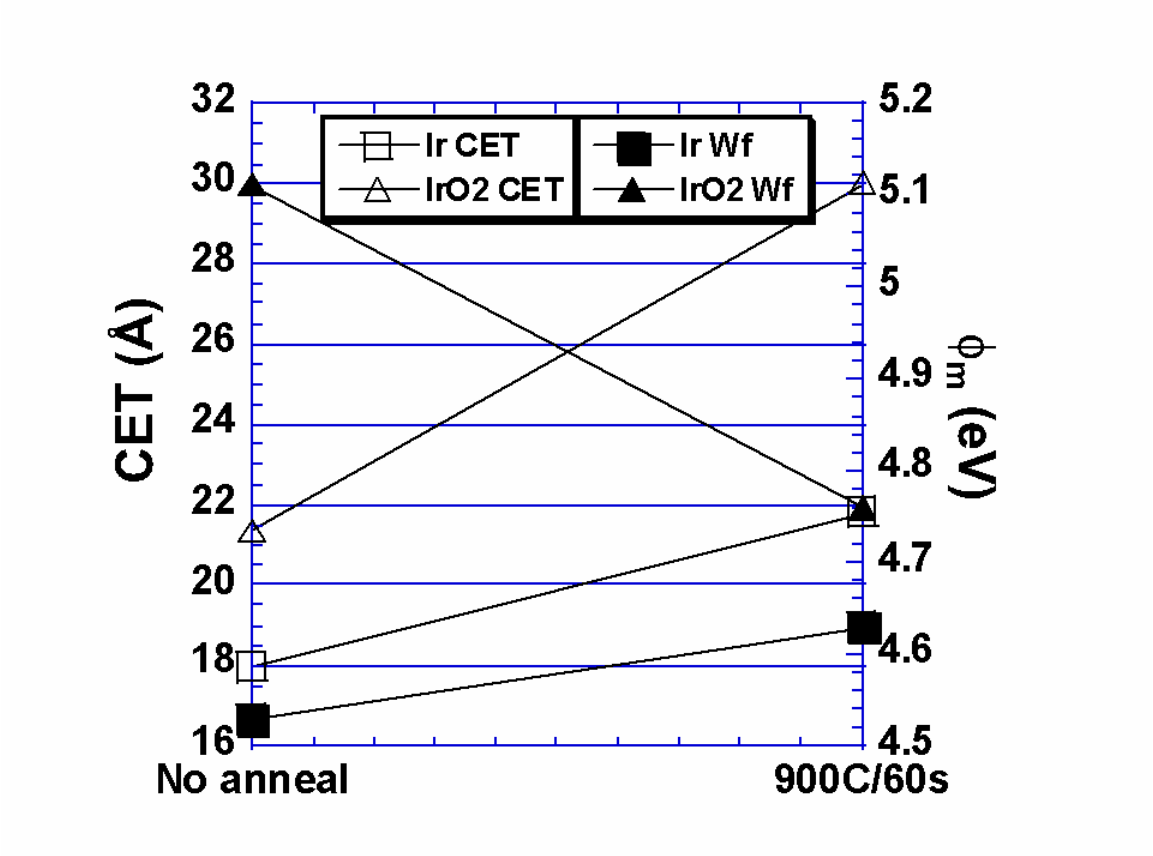

Figure 4.12: Work-function and CET variation in Ir and IrO_2 capacitors as a function of anneal temperature.

Titanium Nitride (TiN) Electrodes

Titanium nitride is another metal gate that has been studied extensively as a mid-gap metal on SiO_2 MOSFETs.[174] TiN films have been sputter deposited, and have a poly-crystalline microstructure as-deposited. Unlike the Ta-Si-N results, the SIMS depth profile for TiN electrodes shows a significant out-diffusion of Hf from the dielectric layer with increased anneal temperature (Fig. 4.13). It is unclear why the Hf out-diffusion occurs, but it can be speculated that the polycrystalline grain structure of TiN enhances the Hf diffusion. The Hf out-diffusion may be part of the reason that a slight increase in interfacial roughness is observed with TEM after annealing (Fig. 4.14). In addition, TiN electrodes consistently result in a lower CET than Ta-Si-N electrodes. Typically, the CET is 1 Å less for TiN electrodes compared to Ta-Si-N electrodes. The CET difference is likely due to differences in sputter damage during the electrode deposition. The TiN deposition power is ~6× greater than the Ta-Si-N deposition power, resulting in sputter removal of approximately 3Å HfO_2 physical thickness as measured with TEM.

The expected MOSFET threshold voltage (V_t) was calculated from TiN/HfO_2 capacitors on N and P substrates as a function of anneal temperature. It was observed that the n-MOSFET V_t from the capacitors with no anneal are much higher than the p-MOSFET V_ts. The reason for this is probably the high negative fixed charge that causes the p-MOSFET V_t to be lower and increases the n-MOSFET V_t. The V_ts become more symmetric with increasing thermal budget. The reasons for this could be one or both of the following: (i) the magnitude of the negative fixed charge decreases, (ii) the work-function of the TiN electrode on HfO_2 decreases. Since varying dielectric thickness splits on different substrates with TiN gates were not explored at different thermal budgets, the exact contribution of the two effects is not known.

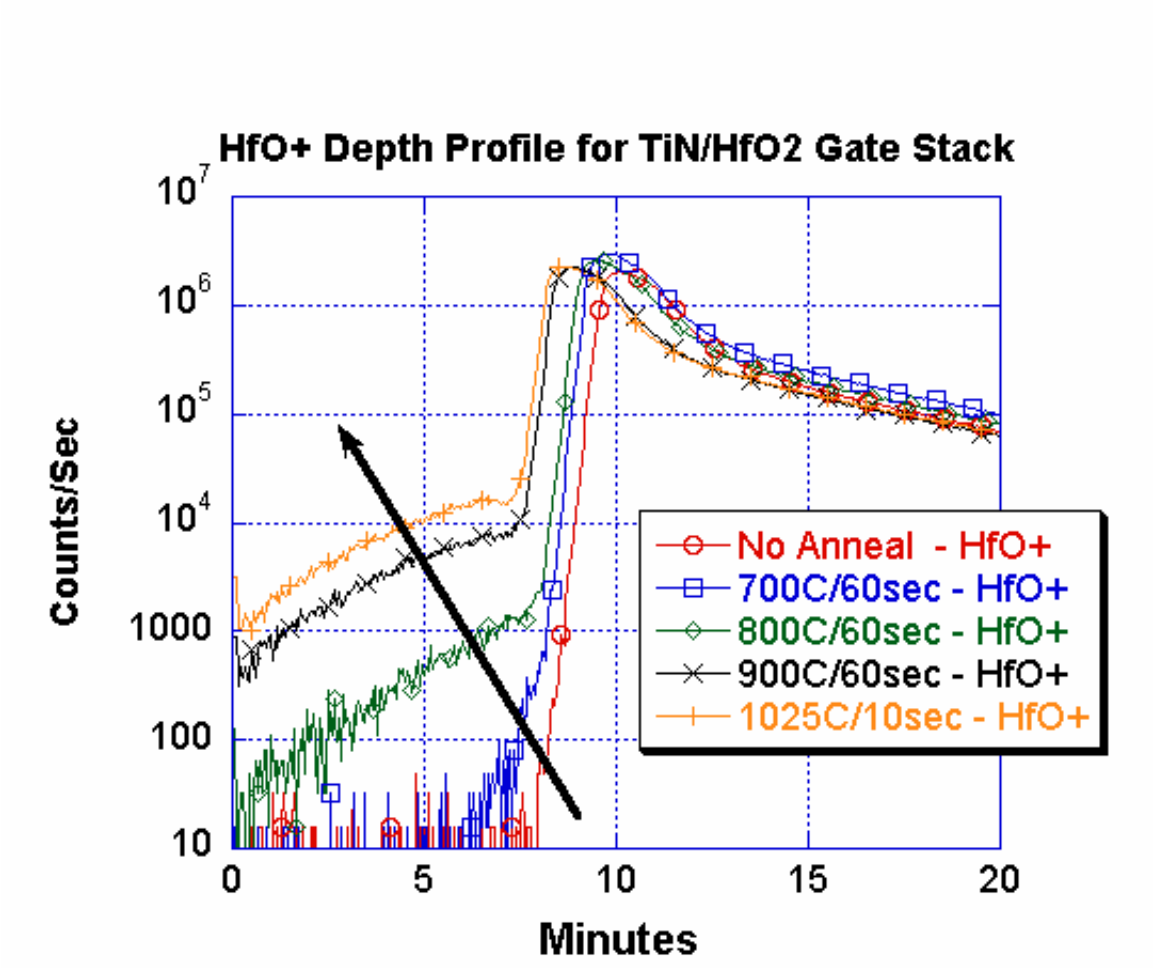

Figure 4.13: SIMS depth profile showing hafnium out diffusion into TiN electrodes with increasing anneal temperature.

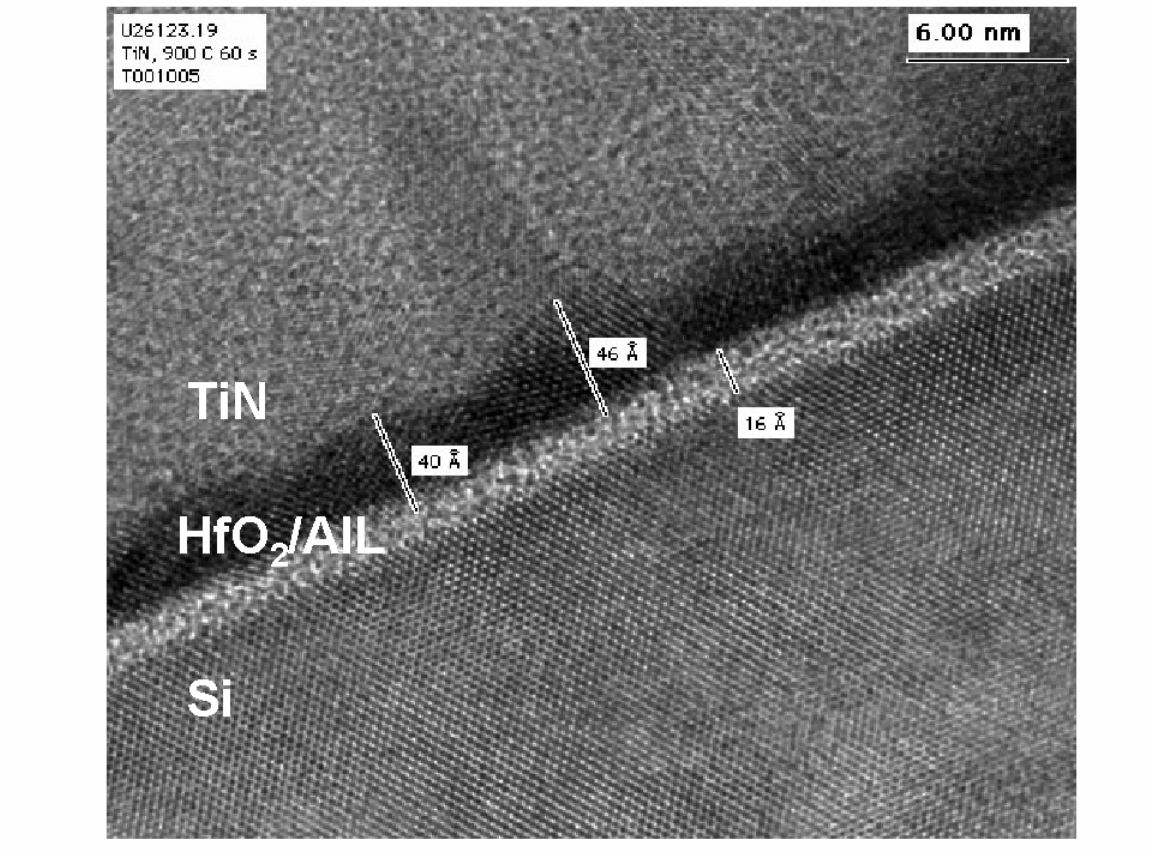

Figure 4.14: TEM of TiN / HfO_2 / Silicon gate stack after a 900°C anneal.

Titanium-Aluminum-Nitride Electrodes

Titanium aluminum nitride electrodes reactively sputtered from an 80:20 Ti:Al target have also been evaluated in contact with HfO_2 dielectrics. In TiAlN the presence of aluminum makes the electrode reactive towards oxygen. TiAlN assumes the rock salt structure characteristic of the interstitial nitrides for Al:Ti ratios <0.40.[175] SIMS depth profiling of a TiAlN/HfO_2 interface reveals a pile-up of aluminum at the interface (Fig. 4b). This is most likely due to the scale growth of an AlO_x layer. This is the same phenomenon that makes this material an effective oxygen diffusion barrier.[176]

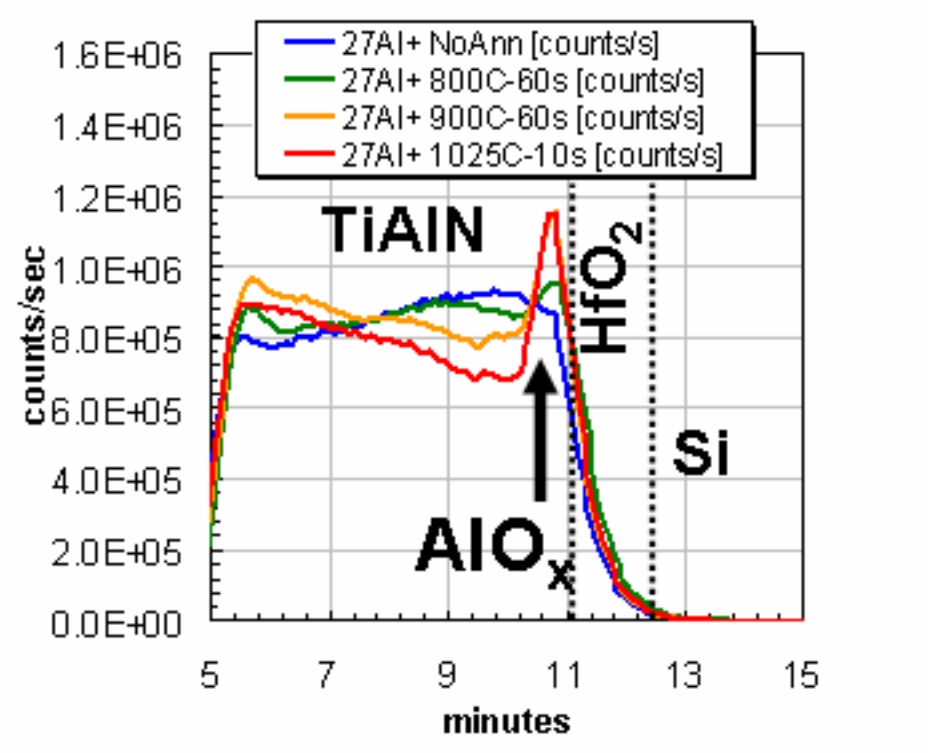

Figure 4.15: SIMS depth profiling of Al+ ion in TiAlN electrodes with varying anneal temperatures.

4.5 DISCUSSION

From this analysis, the amorphous ternary films such as Ta-Si-N exhibit the best interfacial stability in direct contact with HfO_2. Although polycrystalline films such as TiN and TaN exhibit some gate stack inter-diffusion, the amount of inter-diffusion can be minimized by post-deposition treatment of HfO_2. The impact of inter-diffusion on device characteristics warrants further investigation. Some binary films such as WN, TaSi, and IrO_2 exhibit poor phase stability or interfacial reactions at dopant activation anneal temperatures and should be eliminated as candidate materials. One elemental electrode (Ir) has also been evaluated. Gate stack inter-diffusion appears to be a significant issue for iridium electrodes. Platinum and nickel electrodes have been observed to behave similar to iridium electrodes due to similarities in atomic size and electronegativity of these elements.[177] These data show that stability issues exist when weak oxide forming, late transition metals are placed in contact with poly-crystalline HfO_2 and subjected to typical source/drain activation anneal temperatures.

Contrary to the results of the late transition metals, more stable interfaces are obtained using refractory metal compounds, such as interstitial nitrides, where the primary metallic constituent is an early transition metal on the periodic table. In these compounds N occupies octahedral interstices in a face centered cubic metal lattice so that the lattice parameter is typically only ~5% larger than that of the pure metal. Stuffing the interstices with N helps give these materials their excellent diffusion barrier properties. These materials exhibit metal-like conduction, but at the same time are more refractory compared to the pure metal constituent. It is believed that a mixture of metallic, covalent, and ionic bonding character is responsible for this behavior.[178] These common back-end barrier materials appear to be resistant to interfacial reaction and impede gate stack inter-

diffusion. Along with being excellent barrier materials, one reason the early transition metal constituent does not inter-diffuse with HfO_2 is because the more reactive metal species are likely to bind with oxygen at the interface in a TM-O-Hf (TM = transition metal) configuration. This point is further demonstrated by examining the TiAlN/HfO_2 interface, where the presence of aluminum makes the electrode even more reactive towards oxygen.

In summary, it has been speculated that part of the reason early transition metals do not diffuse through the grain boundaries of HfO_2 is because they bind with oxygen at the HfO_2 interface in a TM-O-Hf configuration. Therefore, inter-diffusion is not typically observed when evaluating compounds of the stronger oxide forming metals due to their higher affinity for oxygen. However, weak oxide forming metals are more likely to penetrate through the HfO_2 grain boundaries and react with the substrate. A propensity for inter-diffusion through HfO_2 has been observed with Ni, Pt, and Ir based electrodes at temperatures over 700°C.

Figure 4.16 shows the gate leakage current at 1 V beyond V_{fb} as a function of *CET* for different metal gates on HfO_2/n-Si. All data follow a similar leakage vs. CET trend. Figure 4.17 shows the calculated NMOS and PMOS V_ts for different metal gates on HfO_2 explored in this study. The data is from gate stacks with a 900°C/60s post-gate anneal. It is clear that only Ta-Si-N and TaN appear to be promising as replacements for n+poly in n-MOSFETs. None of the metals evaluated in this study have shown promise as PMOS candidates. Most of the V_{fb} vs. T_{ox} data for PVD metal gates on HfO_2 evaluated in this study show a positive slope suggesting negative fixed charge. The calculated charge density, assuming that it is located at the HfO_2/Si interface, is ~10^{12}/cm^2. Some problems observed in metal gate/HfO_2 systems include variations in CET and work function with increasing thermal budget. Such variations may be due to interfacial electrode/oxide

reactions or to growth of the SiO_2 interfacial layer between the HfO_2 and silicon substrate.

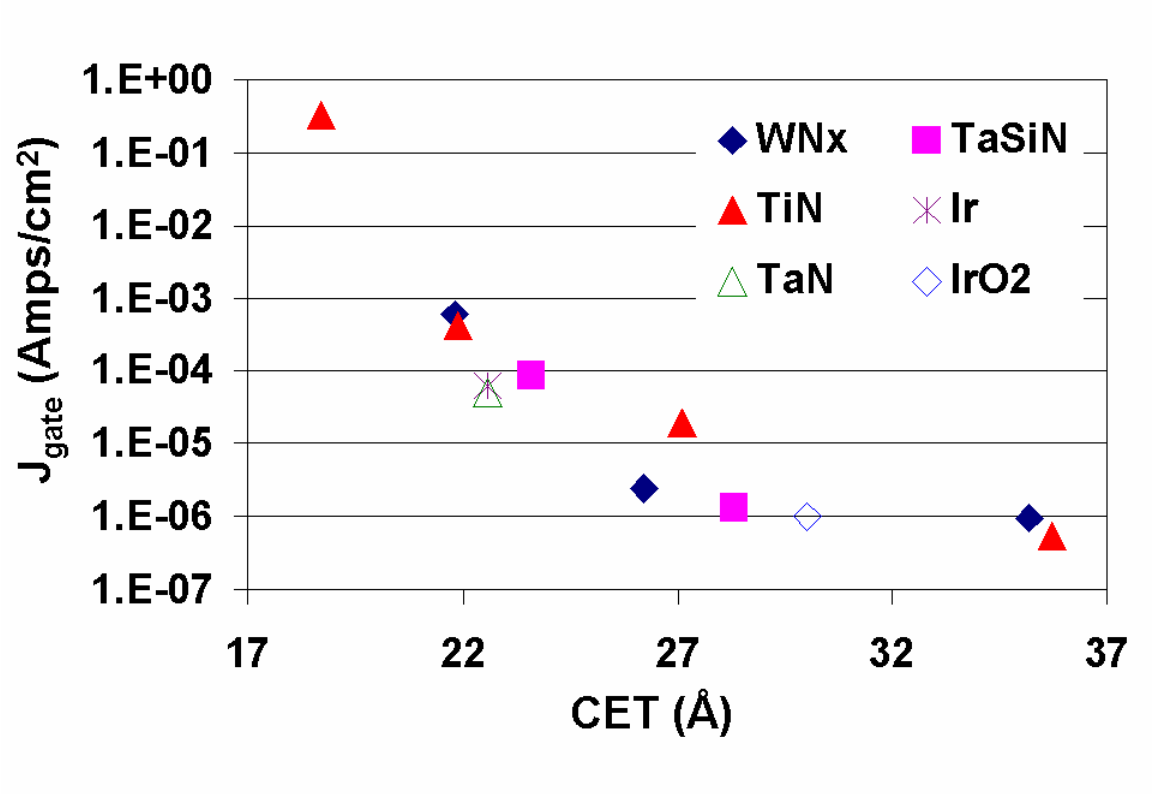

Figure 4.16: Gate leakage at 1V beyond V_{fb} as a function of capacitor CET for different metal gates on HfO_2/n-sub Si. All stacks had a 900°C/60s post-gate anneals.

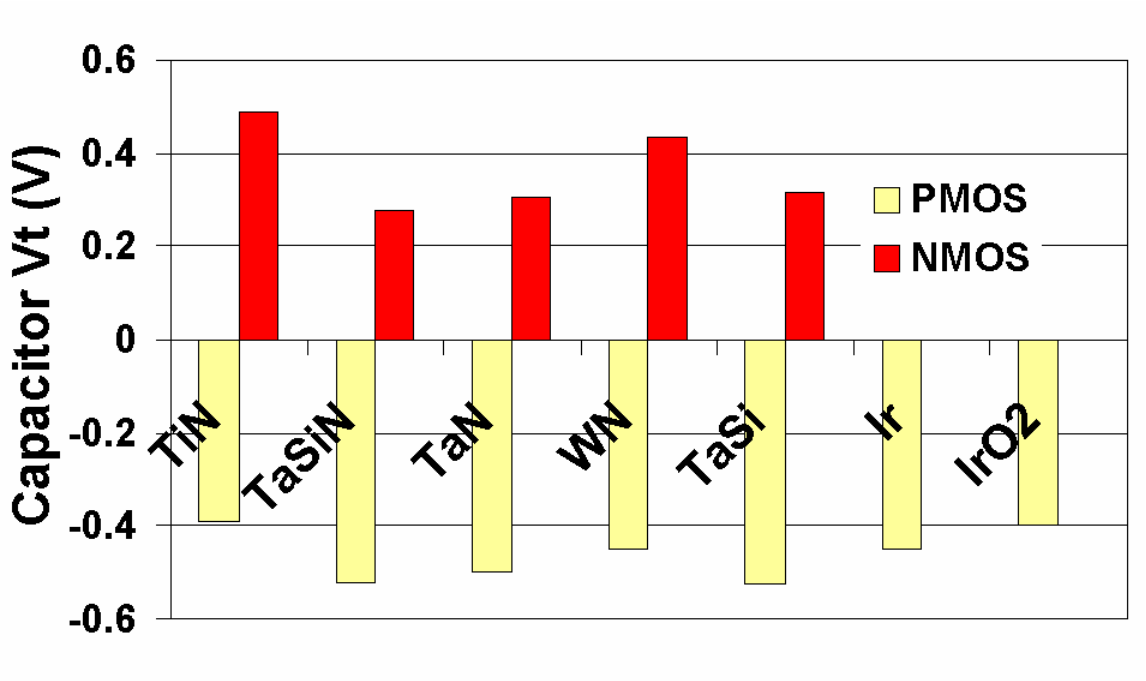

Figure 4.17: NMOS and PMOS V_ts of metal gated-HfO_2 devices estimated from capacitor measurements. All capacitors had a 900°C/60s post-gate anneal.

This comprehensive study of various metal gate electrodes in contact with HfO_2 gate dielectrics elucidates which classes of materials should be considered as strong candidates for metal gate electrodes. Obviously, the amorphous ternary metal nitrides are strong contenders due to their thermal stability in contact with HfO_2. Unfortunately, very little data exist on the work functions of such ternary metals. An entire class of highly metastable amorphous materials exists that satisfies the thermal stability requirements for metal gate electrodes. Some polycrystalline interstitial nitride films appear promising for metal gate applications also. Based on this study, elemental electrodes will likely suffer from interfacial reactions or excessive chemical diffusion and are therefore poor metal gate electrode candidates.

Additional emphases on work function engineering and integration schemes will be critical for realizing CMOS with dual metal gate electrodes. Work function engineering via alloying[179] and dual gate integration by diffusing nitrogen into a metal electrode from a nitrogen rich cap layer[180,181] are two techniques being pursued to achieve low NMOS and PMOS threshold voltages and dual metal gate integrations.

4.6 CONCLUSIONS

Metal gates with work-functions within 0.2 eV of the Si band-edges will be needed for poly replacements. Ta-Si-N, TaN, TaSi, WN, Ir, IrO_2 and TiN were evaluated as gate electrodes for HfO_2 CMOS. Interactions between metal electrodes and HfO_2 were studied where the electrodes are composed of strong or weak oxide forming species. Electrodes comprised of weak oxide forming transition metals demonstrate a propensity to inter-diffuse through the poly-crystalline HfO_2 dielectric. This is loosely attributed to a grain boundary diffusion mechanism. Contrasting this result, stronger oxide forming species do not inter-diffuse into HfO_2. It is believed that the stronger oxide forming

transition metals bind with oxygen at the HfO_2 surface, thus are not free for grain boundary diffusion. The variations of measured work-function and *CET* with thermal budget are issues that need to be evaluated for every gate stack. Inter-diffusion and reactivity at the metal/HfO_2 interface can cause the above variations. Of the metals evaluated, Ta-Si-N and TaN appear promising for n-MOSFETs. Ta-Si-N MOSFETs have been successfully fabricated.[182] None of the metals evaluated have work-functions suited for p-MOSFETS.

Chapter 5: Contributions to the Fermi Level Pinning of Platinum on HfO_2

5.1 ABSTRACT

The intrinsic and extrinsic contributions to Fermi level pinning of platinum electrodes on HfO_2 gate dielectrics are investigated by examining the impact of oxygen and forming gas anneals on the work function of platinum-HfO_2-silicon capacitors. The extracted platinum work function is ~4.6 eV when annealed in forming gas. However, diffusion of oxygen to the Pt/HfO_2 interface increases the platinum work function to a value of ~4.9 eV. Subsequent annealing in forming gas returns the platinum work function to a value comparable to that measured prior to the oxygen anneal. The extracted platinum work functions are compared to the prediction of the metal induced gap states (MIGS) model. The presence of interfacial oxygen vacancies or Pt-Hf bonds is believed to be responsible for a degree of pinning that is stronger than predicted from the MIGS model alone.

5.2 INTRODUCTION

A roadblock to successful implementation of metal gate electrodes with the proper work functions is Fermi level pinning. Fermi pinning is a consequence of forming an interface between a metal and a dielectric (or semiconductor). When an interface is formed, the effective metal work function becomes "pinned" at a different energy than its vacuum work function. This results from interfacial charge exchange between the metal Fermi level and gap states at the metal-dielectric interface causing it to shift with respect

to its unpinned location. A review of Schottky barrier concepts and Fermi level pinning was discussed in Section 1.4.

Recently, Fermi level pinning of poly-Si[183] and metal electrodes[184,185] on HfO_2 has been investigated. However, it was not until after an experiment by Hobbs, et al., that Fermi level pinning gained acceptance as the origin of the elevated threshold voltages observed in poly-Si gated HfO_2 gate dielectrics. To investigate Fermi level pinning as a possible source of the elevated threshold voltages Hobbs, et al. deposited sub-monolayers of HfO_2 on the surface of a 23 Å thermally grown SiO_2 gate dielectric (Fig. 5.1).

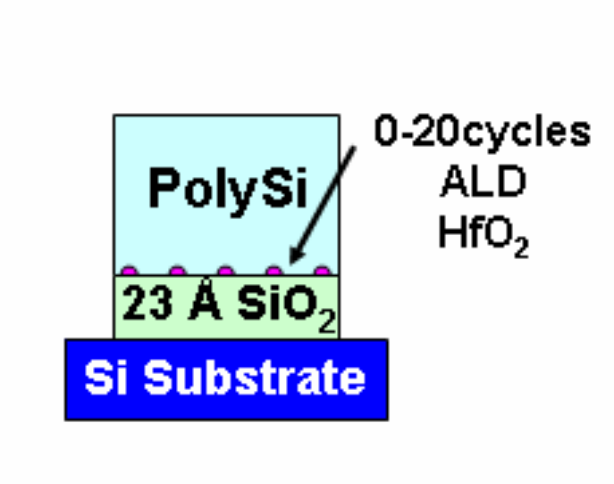

Figure 5.1: Schematic showing the experimental technique used by Hobbs, et al. to study the Fermi level pinning of poly-silicon electrodes on HfO_2.

Atomic layer deposition (ALD) was used to deposit the sub-monolayers of HfO_2. In ALD the substrate is exposed to alternating and sequential pulses of $HfCl_4$ and H_2O precursors. Starting with a hydroxylated surface, film growth proceeds by chemisorption of $HfCl_4$ and H_2O through ligand substitution reactions with the previously chemisorbed species. This process repeats to grow HfO_2 films. Excellent reviews of ALD exist.[186] Hobbs showed with vapor phase decomposition – inductively coupled plasma mass spectroscopy (VPD-ICPMS) that complete HfO_2 surface coverage is not achieved until ~20 cycles (one cycle = one $HfCl_4$ and one H_2O pulse) of ALD growth is complete. This is due to non-uniform film nucleation in the early stages of growth or due to steric hindrance restrictions from the Cl ligands on $HfCl_4$.[187] When analyzing poly-Si/HfO2/n-type Si capacitors Hobbs, et al. report monotonic shifts in the flat band voltage of poly-Si with increasing HfO_2 surface coverage (Fig. 5.2). Flat band voltage shifts are observed with only one cycle of ALD HfO_2, and the shifts saturate at approximately 20 cycles, or when complete surface coverage is obtained. This indicates that the origin of the V_{fb} shift is likely due to increasing the poly-Si/HfO_2 interfacial area, and not due to trapped charges in the HfO_2 dielectric.

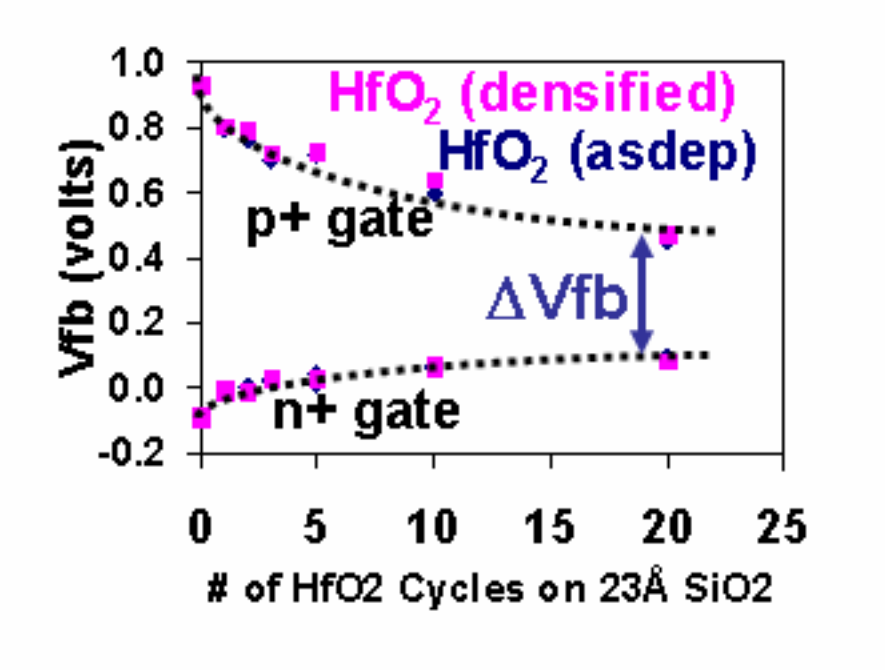

Figure 5.2: V_{fb} shifts as a function of ALD precursor cycles for HfO_2 growth. The shifts tend to saturate when complete HfO_2 surface is obtained.

This experiment demonstrated that the n+ and p+ poly-Si work functions are attracted towards a characteristic energy level. Recall from Section 1.4 that in the MIGS theory this characteristic energy level is referred to as the charge neutrality level (CNL). Plotting the extracted poly-Si work functions (Fig. 5.3) instead of V_{fb} indicates that the 5.2eV and 4.1eV work functions of p+ and n+ poly-Si, respectively, are pulled to an energy in the band gap of silicon of approximately 4.4eV. This value can be considered the experimentally determined charge neutrality level for ALD HfO_2. When sub-monolayers of Al_2O_3 dielectric is used in the same experiment, a charge neutrality level closer to the valence band edge of silicon at a value of approximately 4.9 eV is obtained. This is demonstrated by relatively smaller shifts in V_{fb} for p+ poly-Si (~5.2 eV) and relatively larger shifts for n+ poly-Si (~4.1 eV), where the opposite was observed for the case of HfO_2 sub-monolayers.

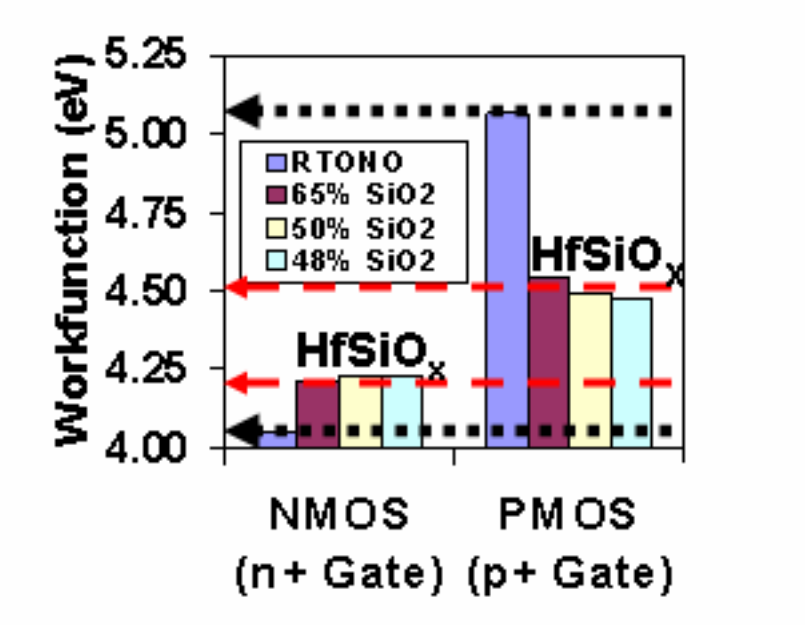

Figure 5.3: Work function of p+ and n+ poly-Si when deposited on SiO_2 and hafnium silicate of various HfO_2:SiO_2 ratios.

Samavedam, et al.,[188] have performed similar experiments to evaluate Fermi pinning with metal instead of poly-Si gate electrodes. In this work relatively modest shifts of ~0.1 V were observed in the flat band voltage for TaSiN electrodes deposited on HfO_2, and larger shifts of ~0.4 V were observed for TaSiN electrodes deposited Al_2O_3. The small V_{fb} shift observed on HfO_2 is due to the fact that TaSiN has a vacuum work function very close to the CNL of HfO_2 of 4.47eV, determined from ultraviolet photoelectron spectroscopy measurements. TiN PMOSFETs and TaN NMOSFETS were also investigated in this study. In general, the work by Samavedam, et al. lends further credence to the argument that the elevated threshold voltages observed in high-κ devices is due to Fermi level pinning.

An important inference from the work of Hobbs and Samavedam is that the charge neutrality level of the dielectric does not depend on the particular metal-dielectric interface in question, but is instead an intrinsic property of the dielectric. Both these studies indicate that the charge neutrality level of Al_2O_3 exists closer to the valence band edge (~4.9 eV) and the CNL of HfO_2 exists at about 4.5 eV regardless of the electrode. This is a pertinent feature of the MIGS theory.

Since Fermi level pinning complicates the effort to find metals with work functions in contact with high permittivity gate dielectrics, further experiments to advance our knowledge of the electrode-HfO_2 interface and Fermi level pinning are necessary. The presence of a dielectric dependent work function muddles the results from other researchers since different dielectrics are being grown by different research groups. Thus, with the exception of fortuitously encountering metal gate electrodes that produce the proper work functions in contact with HfO_2, further experimentation on Fermi level pinning is required.

The metal gates employed in the investigation by Samavedam, et al. employed metals with vacuum work functions at or near the mid-gap of silicon. To better understand the magnitude and the origins of Fermi level pinning on HfO_2; it is important to study materials that possess vacuum work functions well outside the conduction and valence bands of silicon. LaB_6 and Pt satisfy these criteria and have vacuum work functions of 2.9 eV and 5.6 eV, respectively. These work functions are further away from the experimentally determined charge neutrality level of ~4.4 eV for HfO_2 reported in previous investigations. The larger vacuum work functions should allow for more accurate extractions of the pinning parameter (S) for HfO_2. In fact, LaB_6 is commonly used in electron emitter applications because of its exceptionally low work function. Platinum, on the other hand, has one of the highest work functions of all the elemental metals.

5.3 EXPERIMENT

An experiment using platinum electrodes was designed to understand the magnitude and the origins of Fermi level pinning of metals on HfO_2 gate dielectrics. Capacitor stacks consisting of 50 nm tungsten (W), 15 nm titanium nitride (TiN), and 20 nm platinum (Pt) films deposited on a thickness series of hafnium dioxide (HfO_2) were investigated. The HfO_2 films were produced by atomic layer deposition (ALD) with 4 nm, 6 nm, 8 nm, and 10 nm physical thicknesses with each sample receiving a 500°C anneal for 60 seconds in O_2 following the dielectric deposition. The thickness series of HfO_2 allows us to extract the work function of the platinum electrode by plotting the capacitor flat band voltage (V_{fb}) versus the effective oxide thickness (EOT) of the HfO_2 film. Since $V_{fb} = \phi_{ms} - Q_f \times EOT/\varepsilon_{SiO2}$, where Q_f is the oxide fixed charge and ε_{SiO2} is the permittivity of silicon dioxide, the slope in the V_{fb} vs. EOT plot gives the magnitude and

sign of the oxide fixed charge and the intercept provides the work function potential difference, ϕ_{ms}. This equation assumes that all the oxide fixed charge exists at the dielectric/silicon interface. Since $\phi_{ms} = \phi_{m,eff} - \phi_s$, where ϕ_s is the Fermi energy of the silicon, the effective metal work function, $\phi_{m,eff}$, can be calculated. V_{fb} and EOT values were extracted by fitting capacitance-voltage curves of MOS capacitors to the CVC program.[189]

Three thickness series of HfO_2 films were investigated with a different anneal condition for each. In the first thickness series, W/TiN/Pt/HfO_2 films were deposited and plasma etched to form capacitors. The capacitors were annealed in forming gas at 450°C for 30min (Fig. 5.4.a.). For the second thickness series, blanket HfO_2 and Pt films were deposited and a 500°C oxygen anneal was performed for 60 seconds. The W/TiN cap was then deposited, followed by electrode patterning and etch. No forming gas anneal was performed on these films (Fig. 5.4.b). The third condition is identical to the second except the samples were annealed in forming gas at 450°C for 30min after the gate etch (Fig. 5.4.c). For simplicity, these three conditions are referred to as FG ONLY, O_2 ONLY, and O_2+FG, respectively.

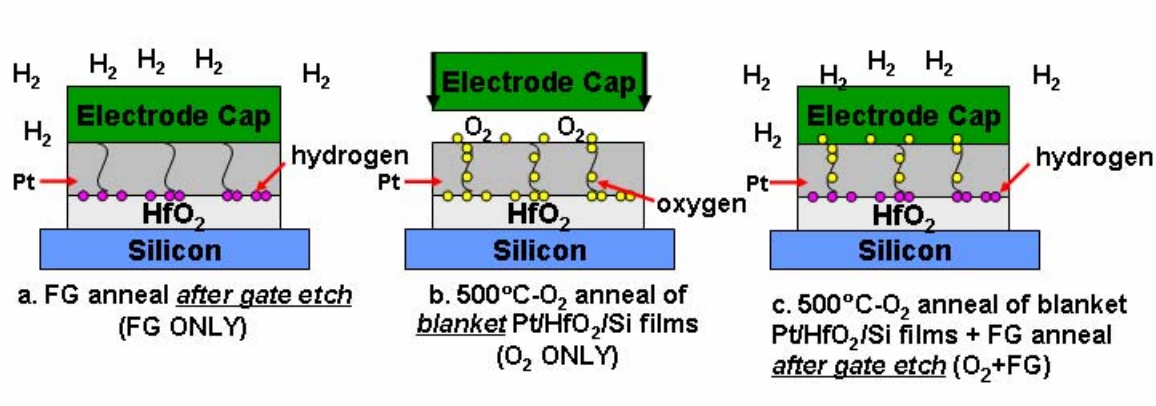

Figure 5.4: Different capacitor stacks fabricated to evaluate the work function of platinum

Platinum was selected as the gate electrode because oxygen diffuses through thin platinum films (< 20nm) via a grain boundary diffusion mechanism at low temperatures[190] and platinum does not oxidize at 500°C. These characteristics enable the diffusion of oxygen to the HfO_2 without bulk chemical modification of the electrode. It should be noted that platinum is reported to be stable on HfO_2 at 500°C.[191] This investigation validates this result, but indicates that the Pt/HfO_2 interface does not demonstrate interface stability at temperatures approaching 700°C. The high vacuum work function of platinum is also sufficiently far from the empirical charge neutrality level of ALD HfO_2 films (~4.4 eV) as to have a certain degree of confidence in our extracted values of the Schottky pinning parameter (*S*).

5.4 RESULTS AND DISCUSSION

Secondary ion mass spectroscopy (SIMS) was performed on the three gate stacks to verify the diffusion of oxygen through platinum to the HfO_2 interface (Fig. 5.5). This data indicates that the O_2 ONLY anneal successfully drives oxygen to the Pt/HfO_2 interface. The oxygen concentration is approximately one order of magnitude higher than that of the FG ONLY condition at the Pt/HfO_2 interface. The O_2+FG sample shows an oxygen depth profile similar to the profile obtained from the O_2 ONLY condition indicating that oxygen remains in the platinum even after a subsequent forming gas anneal. In addition, negligible differences were observed when comparing the oxygen depth profiles in the HfO_2 for all three anneal conditions. SIMS does not provide sufficient depth resolution to distinguish differences in the oxygen concentration precisely at the Pt/HfO_2 interface. An examination of the samples using transmission electron microscopy revealed no changes of the various interfaces due to any of the annealing conditions (Fig. 5.6).

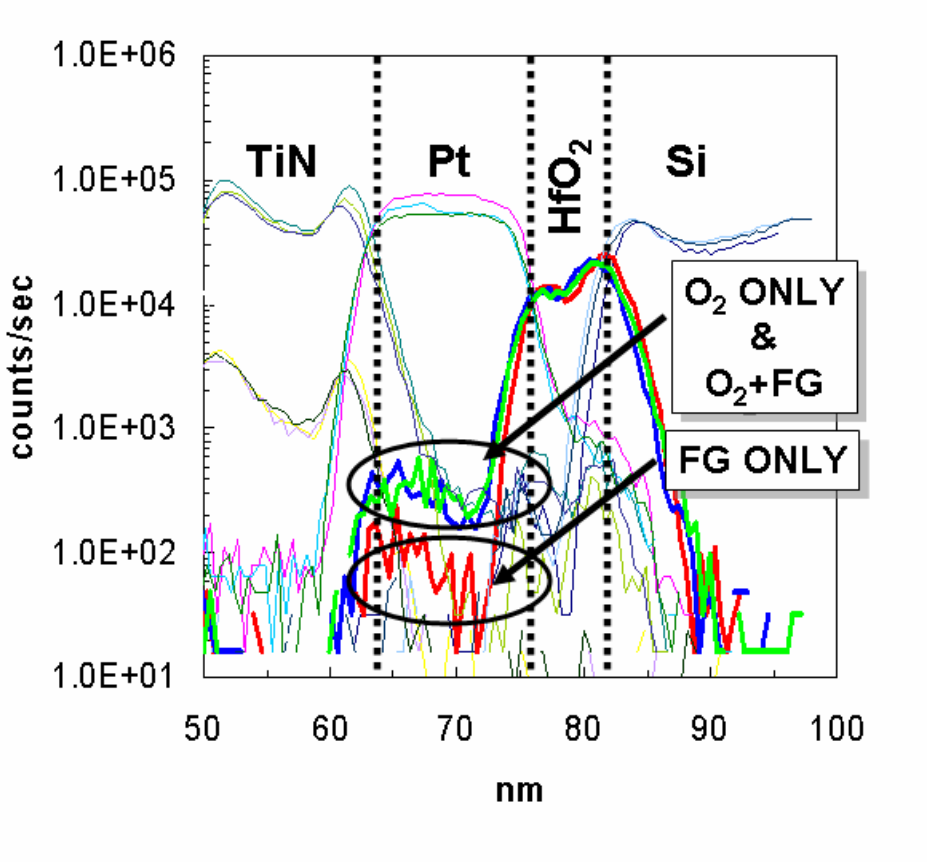

Figure 5.5: SIMS depth profile showing TiN/Pt/HfO2/Si layers. Bold lines represent the oxygen depth profiles.

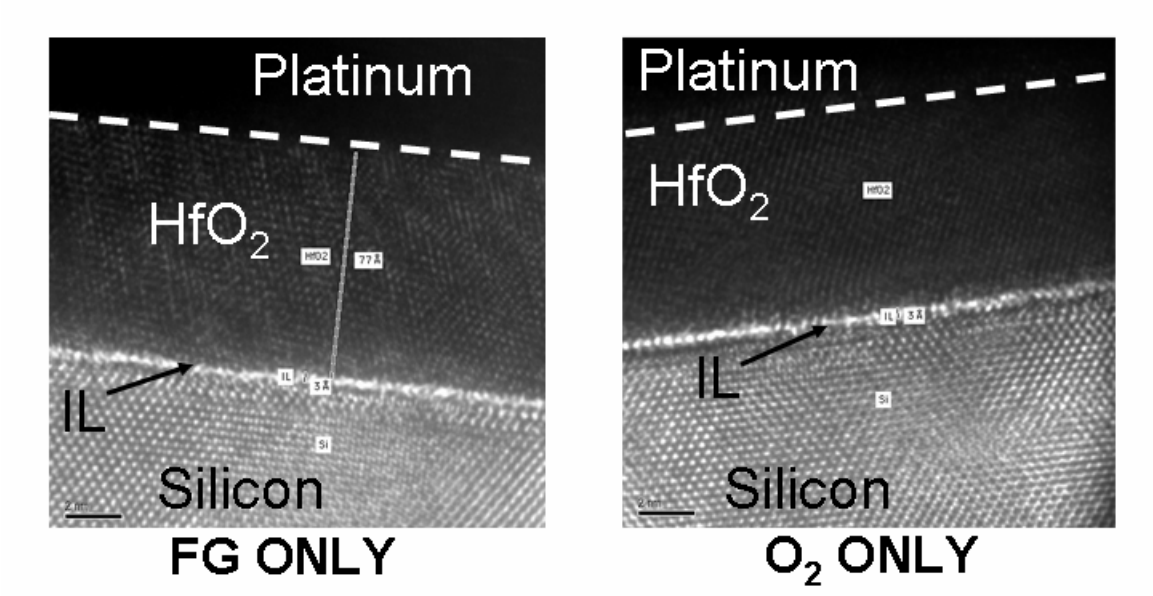

Figure 5.6: Pt/HfO_2/Si stacks for the FG ONLY and the O_2 ONLY conditions. HfO_2 thickness is ~80 Å and the IL thickness is ~3 Å for both conditions.

The experiment was conducted twice to verify the initial result. In the first experiment, the capacitor area was 100 μm × 100 μm with a well doping concentration of $2\times10^{15}/cm^3$ (ϕ_s = 4.30 eV). A plot of *EOT* vs. V_{fb} for the first experiment reveals that ϕ_{ms} is ~0.25 eV higher for the O_2 ONLY split than for the FG ONLY or the O_2+FG splits (Fig. 5.7). Effective work function (fixed charge) values are 4.56 eV ($-2.34\times10^{12}/cm^2$), 4.87 eV ($+1.09\times10^{12}/cm^2$), and 4.59 eV ($-1.48\times10^{12}/cm^2$) for the FG ONLY, O_2 ONLY, and O_2+FG conditions, respectively (Figs. 5.8 and 5.9). In this experiment the O_2 ONLY anneal results in a sign change from negative to positive for the oxide fixed charge.

The second experiment employed 85 μm × 80 μm capacitors and a well doping concentration of $5\times10^{17}/cm^3$ (ϕ_s = 4.14 eV). For this experiment the oxide fixed charge is negative for all samples, but ϕ_{ms} is again ~0.25 eV higher for the sample with the O_2 ONLY anneal than for the FG ONLY and the O_2+FG anneals (Fig. 5.7). The effective work function (fixed charge) values from the second experiment are 4.67 eV ($-3.11\times10^{12}/cm^2$), 4.87 eV ($-3.52\times10^{12}/cm^2$), and 4.55 eV ($-4.79\times10^{12}/cm^2$) for the FG ONLY, O_2 ONLY, and O_2+FG conditions, respectively (Figs. 5.8 and 5.9).

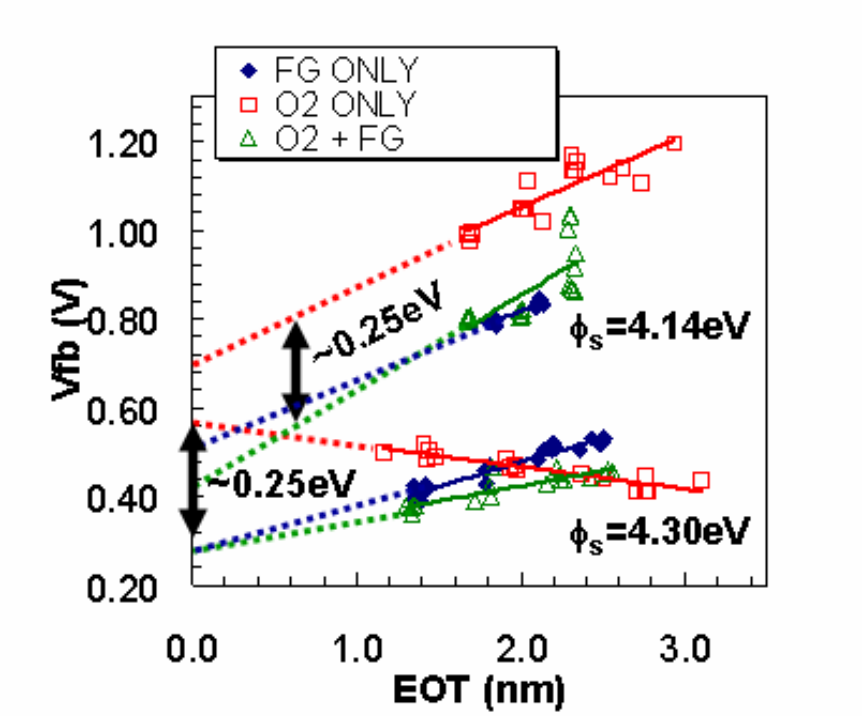

Figure 5.7: Plot of effective oxide thickness (*EOT*) vs. flat band voltage (V_{fb}) with substrate doping of $2\times10^{15}/cm^3$ (ϕ_s = 4.30 eV, bottom grouping) and $5\times10^{17}/cm^3$ (ϕ_s = 4.14 eV, top grouping).

Both experiments indicate that diffusion of oxygen through the platinum to the HfO_2/Pt interface increases the platinum work function, and that a subsequent forming gas anneal returns the work function to a value similar to that extracted when the oxygen anneal is never performed. The same anneals did not produce measurable differences in the vacuum work function of the platinum surface from ultraviolet photoelectron spectroscopy (UPS) studies, suggesting that the work function modulation is due to changes at the Pt/HfO_2 interface. Platinum samples annealed at the FG ONLY, O_2 ONLY, and O_2+FG conditions have UPS work functions of 5.6 eV.

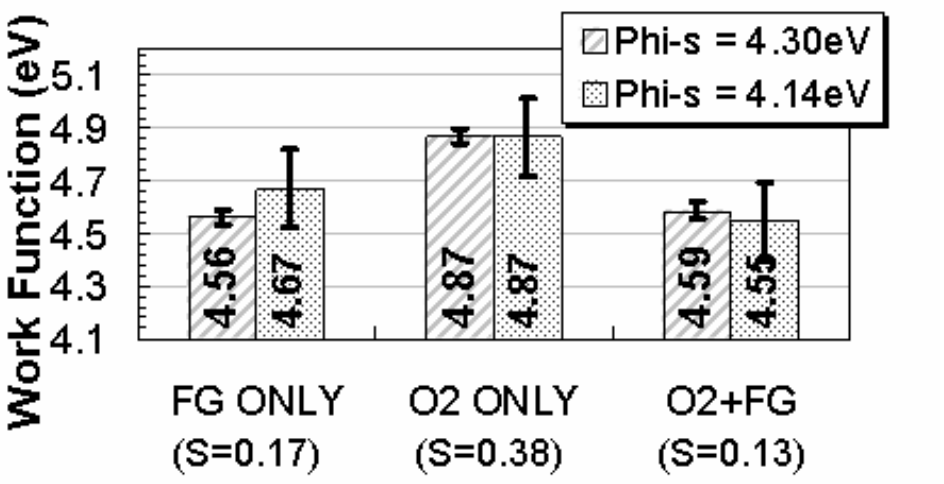

Figure 5.8: Platinum work functions for the three anneal conditions. The average pinning parameter (*S*) is provided under the x-axis label. The 95% confidence levels are indicated by error bars.

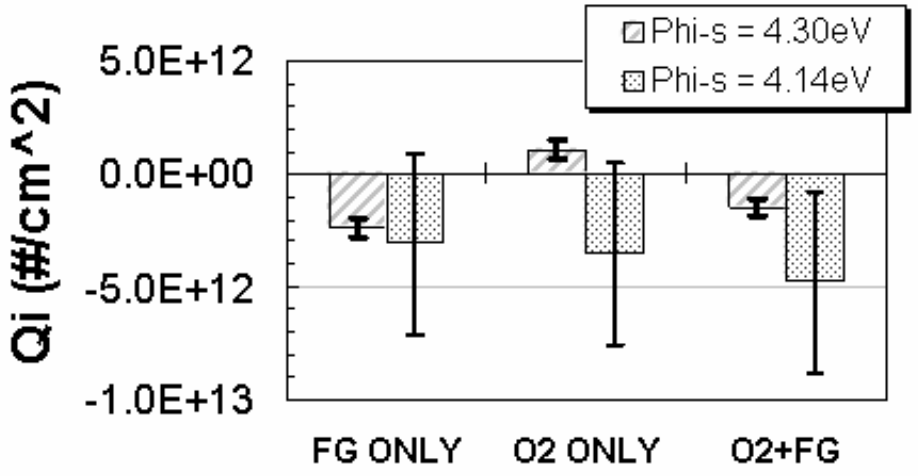

Figure 5.9: Oxide fixed charge (Q_i) for the three anneal conditions. The 95% confidence levels are indicated by error bars.

The fact that the effect of the O_2 anneal can be reversed with a subsequent forming gas anneal illuminates the physical phenomena which might be responsible for these effective work function variations. Recalling the SIMS results where a forming gas anneal shows no measurable impact on the oxygen concentration in the platinum, the effective work function differences are possibly due to modifications of the Pt/HfO_2 interface electronic dipole. Chemical modification of interface dipoles has previously been extensively studied in the fabrication of metal-insulator-semiconductor gas sensors using catalytically active platinum and palladium electrodes with SiO_2 and Si_3N_4 gate insulators.[192,193,194] Numerous studies on this subject report changes in V_t, V_{fb}, and $\phi_{m,eff}$ upon exposure of the heated capacitor element to various chemical environments. In fact, cyclic changes to $\phi_{m,eff}$ have been demonstrated for repeated exposures to H_2 and O_2 ambients.[193]

This study shows similar phenomena, but the results can also be analyzed to provide information on the physical nature of the extrinsic defects that contribute to Fermi level pinning of metals deposited on HfO_2. Figure 5.8 shows the work function obtained for each anneal condition and the pinning parameter (S) provided that $\phi_{m,vac}$ = 5.6 eV for platinum (measured using UPS) and ϕ_{CNL} = 4.4 eV for HfO_2 (measured using poly-Si electrodes). Using these numbers and our extracted effective work function values, S is approximately 0.15 for the two forming gas last anneal conditions, and approximately 0.38 for the O_2 ONLY anneal condition. The O_2 ONLY anneal condition is closer to the Schottky pinning parameter for HfO_2 of S=0.53 as calculated from the electronic component of the dielectric constant, ε_∞.[195] This comparison of the experimental and theoretical pinning strengths of HfO_2 suggests that extrinsic states exist at the Pt/HfO_2 interface and that their pinning contribution is minimized in the O_2 ONLY condition.

It is likely that oxygen diffusion to the Pt/HfO_2 interface occurs predominantly through the platinum grain boundaries. When the oxygen diffuses to the Pt/HfO_2 interface, oxygen vacancies (V_O) or Pt-Hf interface bonds are believed to be reduced in concentration. The addition of oxygen can modify the proportion of charge exchanged at the Pt/HfO_2 interface. Platinum is more electronegative than hafnium (Hf), thus an interface bonding configuration of Pt-Hf or Pt-V_O-Hf results in electron transfer to Pt reducing $\phi_{m,eff}$ (Fig. 5.10). It is believed that the enhanced presence of the more electronegative oxygen atom attracts electrons from platinum to oxygen, thus lowering the platinum Fermi energy and increasing its effective work function relative to the FG ONLY condition. A similar argument was made for poly-Si/HfO_2 interfaces. These results also indicate that the O_2+FG anneal reverses the impact of the O_2 ONLY anneal. It is suspected that the catalytic nature of the platinum electrode towards the dissociation of H_2 and the sensitivity of the V_O concentration in HfO_2 to the oxygen partial pressure can result in reversible modifications to the interface dipole and $\phi_{m,eff}$. In addition, it has been shown from calculations and UPS studies that a partially reduced HfO_2 surface has states that lie within the HfO_2 band gap.[196] The UPS studies show an elevated density of states near the valence band edge when the HfO_2 surface is reduced with ~1 monolayer of hafnium deposition. These states may contribute to an increased degree of pinning.

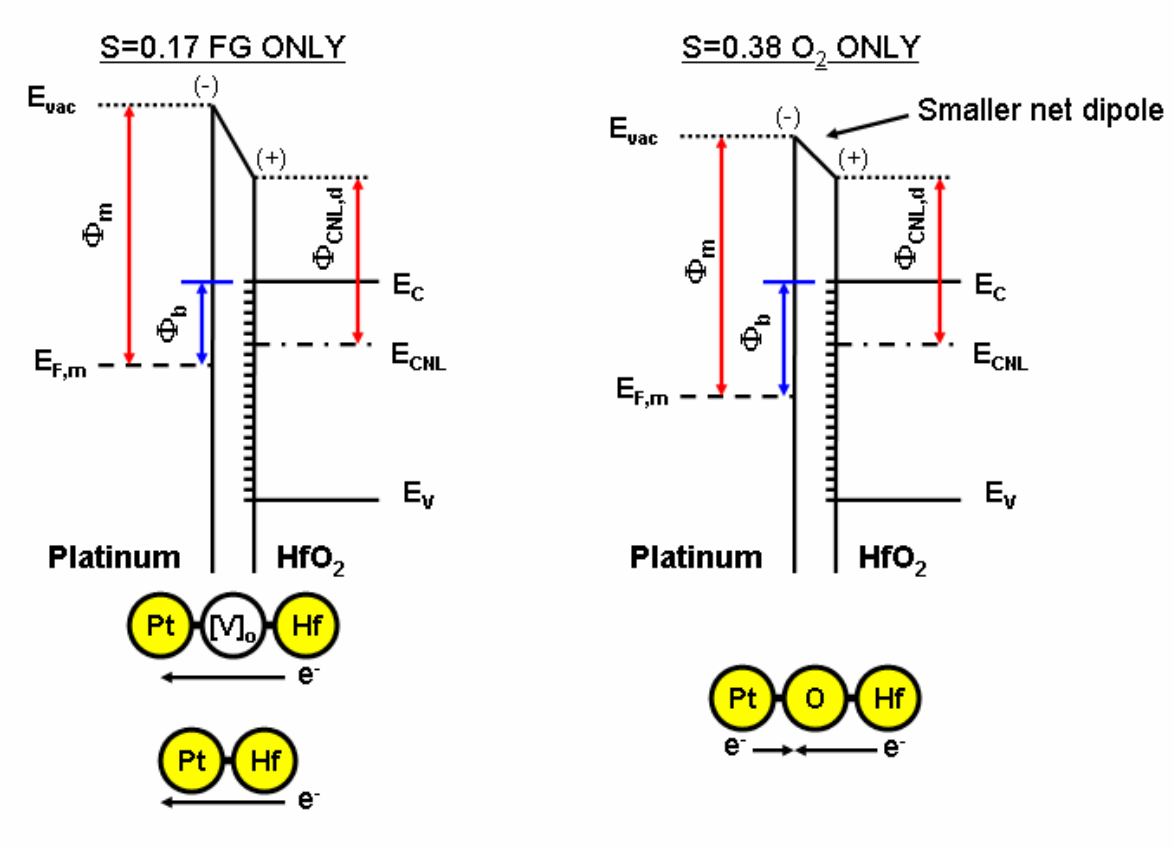

Figure 5.10: Band alignments showing the magnitude of the interfacial dipole for the FG ONLY and the O_2 ONLY anneal conditions. The interface dipole is of atomic dimensions.

Although there is agreement between the extracted work function values, there is a discrepancy between the oxide fixed charge values for the two experiments. It was shown that the oxide fixed charge changes sign with the O_2 ONLY anneal for the experiment with the low well doping (Q_f = +1.09×10^{12}/cm^2), but not for the experiment with high well doping (Q_f = -3.52×10^{12}/cm^2). Since there does not appear to be a correlation between $\phi_{m,eff}$ and Q_f with anneal ambient, the observed work function modulation for both experiments is not easily explained by a redistribution of fixed charges in the dielectric. Thus, we believe the modulation of the effective work function is real. It is also possible that the O_2 anneal has the added effect of reducing the concentration of negative fixed charges present in the dielectric as observed in the experiment with the lower well doping concentration of 2×10^{15}/cm^3.

The experiment with platinum electrodes on HfO_2 advances our understanding Fermi level pinning. Platinum on HfO_2 exhibits a 0.25 eV higher work function when the interface is oxygen-rich. This is attributed to a reduced concentration of extrinsic defects such as oxygen vacancies or Pt-Hf bonds. These defects can be minimized by controlling the process conditions.

To provide better understanding of Fermi level pinning on HfO_2 metals with work functions well below ϕ_{CNL} of HfO_2 also need to be considered. One such metal is LaB_6. LaB_6 is often used in electron emitter applications, such as TEMs, due to its low work function (ϕ_m = 2.55-3.65 eV).[197] LaB_6 was e-beam evaporated on HfO_2 and SiO_2 substrates to evaluate the extent of Fermi level pinning on HfO_2.[198] A plot of V_{fb} vs. EOT for LaB_6 on HfO_2 (Fig. 5.12a) indicates that the effective metal work function is nearly 0.8 eV lower on SiO_2 substrates than on HfO_2 substrates. W/LaB_6/SiO_2/Si capacitor stacks annealed at 800 °C in N_2 for 60sec yield a work function of 3.47 eV. In contrast, W/LaB_6/HfO_2/Si stacks annealed at 390 °C for 30min in forming gas, 800 °C in N_2 for

60sec, and 900 °C in N_2 for 60sec produce work functions of 4.46 eV, 4.31 eV, and 4.21 eV, respectively. SIMS and TEM analysis indicate diffusion of LaB_6 through the HfO_2 and reaction with the substrate for a 900 °C anneal. This was not detected for annealing temperatures ≤800°C. For low work function materials, electrons are exchanged from the LaB_6 to the charge neutrality level of the HfO_2 creating an interface dipole in the opposite direction from the Pt/HfO_2 experiment (Fig. 5.12b). The extracted pinning parameter for LaB_6 in contact with HfO_2 is approximately S = 0.1. This value is similar to that of Pt with a FG anneal.

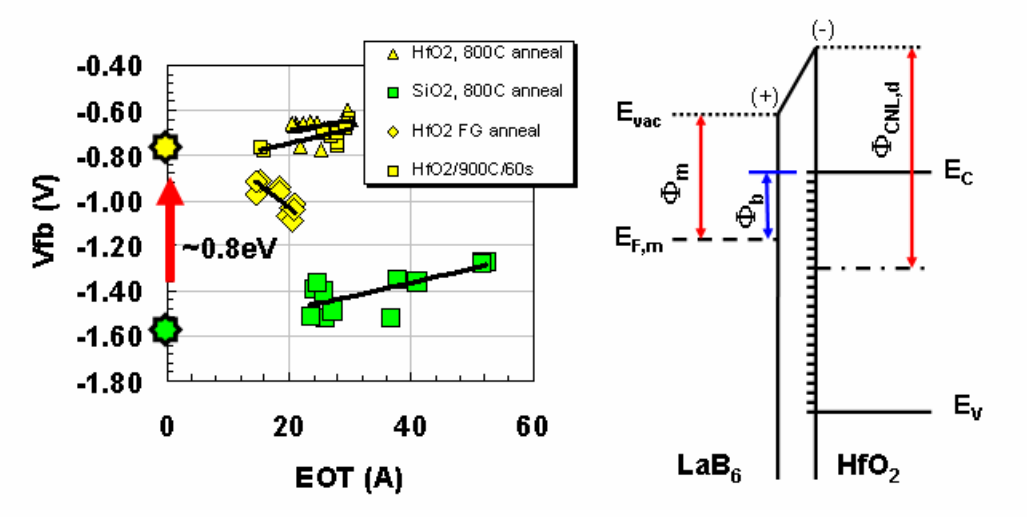

Figure 5.11: V_{fb} vs. *EOT* for W/LaB_6/HfO_2/Si capacitors (left) and schematic showing the interface dipole formation for LaB_6/HfO_2. The interface dipole width is of atomic dimensions.

A brief discussion of the LaB_6 investigation was provided to compliment the platinum electrode study. The LaB_6 investigation gives additional confidence that Fermi level pinning, as explained by the MIGS model, is responsible for the work function pinning. LaB_6 and n+ poly-silicon have work functions that shift upwards towards the experimentally determined charge neutrality level of HfO_2, and Pt and p+ poly-silicon have work functions that shift downwards towards the experimentally determined charge neutrality.

5.5 CONCLUSIONS

In conclusion, LaB_6 and n+ poly-silicon have work functions that shift upwards towards the charge neutrality level of HfO_2, and Pt and p+ poly-silicon have work functions that shift downwards towards the charge neutrality level of HfO_2. This gives credibility to Fermi level pinning, as explained by the MIGS model, as the origin of the elevated threshold voltages for HfO_2 based MOS capacitors. Additionally, an experimental technique for modulating the chemical environment of a buried Pt/HfO_2 interface without modifying the bulk properties of platinum has been established. Grain boundary diffusion of oxygen to the Pt/HfO_2 interface influences the interface dipole and thus the extracted metal work function. Platinum on HfO_2 exhibits a 0.25 eV higher work function when the interface is oxygen-rich. This is attributed to a reduced concentration of extrinsic defects such as oxygen vacancies or Pt-Hf bonds. These defects can be minimized by controlling the process conditions. However, even if extrinsic contributions to Fermi level pinning can be eliminated, the intrinsic component of Fermi pinning may still pose formidable challenges to the implementation of high permittivity CMOS devices with metal gate electrodes.

Chapter 6: Conclusions and Recommendations

6.1 CONCLUSIONS

Three separate, but related, regions of high permittivity gate stacks for advanced CMOS devices have been studied. The first study is an attempt to correlate the physical properties of HfO_2 films to their electrical behavior, where the physical properties are controlled by MOCVD growth and annealing conditions.[199] The second investigation is on metal gate electrodes.[200,201] This investigation provided insight into which metals have thermodynamic stability in contact with HfO_2 and which metals have acceptable effective work functions in contact in CMOS devices. Knowledge from the first two studies was then applied towards a third investigation[202,201] on Fermi level pinning, a phenomena that occurs at the metal-HfO_2 interface. By exploiting some of the bulk and interface properties of HfO_2 and a platinum metal gate, insight into the magnitude of the metal Fermi level pinning and possible extrinsic defects responsible for Fermi level pinning were investigated. Together, the three studies have considered many of the materials properties that are responsible for the electrical behavior at the metal electrode – HfO_2 interface.

In the first study, HfO_2 films grown using TDEAH (tetrakis diethylamido hafnium) precursor were evaluated as candidate high permittivity gate dielectrics. Deposition rates, film microstructure, impurity content, grain diameter, and density are highly dependent on the growth temperature. Increasing the deposition temperature enhances the leakage properties of HfO_2 gate dielectrics. These improvements are likely due to reduced carbon impurity content and higher density films achieved at the 550 ºC deposition temperature. The carbon impurities exist as clusters that degrade the electrical

properties. It appears that when the carbon cluster density or size is reduced past a maximum threshold, dramatic improvements in the electrical characteristics are achieved.

The second study investigated metal gate electrodes with the goal of discovering work functions near the Si band-edges as replacements for n+ and p+ poly-silicon. Ta-Si-N, TaN, TaSi, WN, Ir, IrO_2 and TiN were evaluated as gate electrodes on HfO_2 dielectric. Differences in thermal stability are observed for electrodes comprised of early transition metals and those consisting of late transition metals. In summary, early transition metals do not diffuse through the grain boundaries of HfO_2. One possibility for why this occurs is because they form chemical bonds, binding with oxygen at the HfO_2 interface in a TM-O-Hf configuration. Therefore, inter-diffusion is not typically observed when evaluating electrodes comprised of early transition metals due to their higher affinity for oxygen. However, late transition metals, which are weak oxide formers, are more likely to penetrate through the HfO_2 and react with the substrate. A propensity for inter-diffusion through HfO_2 has been observed with Ni, Pt, and Ir based electrodes at temperatures over 700°C. It is possible that this inter-diffusion occurs through grain boundaries or voids in the HfO_2. Additionally, variations of measured work-function and CET with thermal budget are issues that need to be evaluated for every gate stack. Inter-diffusion and reactivity at the metal/HfO_2 interface can cause the above variations. Of the metals evaluated, Ta-Si-N and TaN appear promising for n-MOSFETs. Ta-Si-N MOSFETs have been successfully fabricated.[203] None of the metals discussed have work-functions suited for p-MOSFETS.

The third study discusses Fermi level pinning, a problem hindering the efforts to find metals with the proper effective work functions in contact with HfO_2. As described within the metal induced gap states framework of Fermi level pinning, LaB_6 and n+ poly-silicon have work functions that shift upwards towards the charge neutrality level of

HfO_2, and Pt and p+ poly-silicon have work functions that shift downwards towards the charge neutrality level of HfO_2. These prior experiments lend credibility to Fermi level pinning, as explained by the MIGS model, as the origin of the elevated threshold voltages for HfO_2 based MOS capacitors. To further explain the origins of these unexpected shifts in effective work function, an experimental technique for modulating the chemical environment of a buried Pt/HfO_2 interface without modifying the bulk properties of platinum was established. Grain boundary diffusion of oxygen to the Pt/HfO_2 interface influences the interface dipole and thus the extracted metal work function. Platinum on HfO_2 exhibits a 0.25 eV higher work function when the interface is oxygen-rich. This is attributed to a reduced concentration of extrinsic defects such as oxygen vacancies or Pt-Hf bonds. These defects can be minimized by controlling the process conditions. However, even if extrinsic contributions to Fermi level pinning can be eliminated, the intrinsic component of Fermi pinning may still pose formidable challenges to the implementation of high-permittivity gate dielectrics.

6.2 RECOMMENDATIONS FOR FUTURE EXPERIMENTS

Although a significant amount of work has already been published on the materials properties of high permittivity gate dielectrics, significant research opportunities still exist. Now that the industry is settling on HfO_2, hafnium silicate, and hafnium silicon oxy-nitride more focused and detail investigations are required. Future research should attempt to bridge the gap between the poor reliability and charge trapping characteristics of HfO_2 and the responsible physical properties. This will require more concerted collaboration between the electrical engineering and solid state device communities with the materials science and solid-state physics communities. Furthermore, such collaborations should even be performed on the same sample sets.

There has recently been an increased interest to examine point defects within HfO_2.[204,205,206] Physical understanding of electrical traps in HfO_2 and their characteristics after electrical stressing are invaluable. Such studies are of the utmost importance to the device community to obtain better understanding of the charge trapping and reliability characteristics of HfO_2. These efforts should lead to new models which will advance our understanding, but undoubtedly be passionately debated in the years ahead.

Regarding the published literature on metal gate electrodes, there is very little consideration given to the physical properties of the metal gate. It is well known that properties such as crystal orientation and stoichiometry can have a dramatic impact on the vacuum work function of metals. Thus, it is likely that the preferred orientation and stoichiometry also impacts the barrier height, or effective work function, at the metal-HfO_2 interface. Because the materials properties of the electrodes have been neglected, sifting through the metal gate literature can be very confusing. Widely varying values of work function have been reported for what is at a superficial glimpse the same metal. Simulations have been performed that indicate the extent to which interface defects or preferred orientation can influence work function, but additional experimental work should also be devoted to this subject. Although there is an industrial scramble to find metals with the proper work functions in contact with HfO_2, some deliberate materials studies should be performed to provide additional fundamental understanding on the interface properties that might influence the work functions of metals in contact with HfO_2. Some recent studies have started to evaluate the local chemistry at the electrode – HfO_2 interface using electron energy loss spectroscopy.[207]

Additional work should also be performed to better understand Fermi level pinning. First, it is possible that the work function extraction technique currently used might be somewhat convoluted by the assumptions made about the fixed charges in the

dielectric. The linear V_{fb} vs. EOT relationship used in this research models all the dielectric fixed charge as if it exists at the Si/HfO_2 interface. However, it is possible that this fixed charge is not uniformly distributed throughout the dielectric. Some charge may exist at the Si/SiO_2 interface, some at the SiO_2/HfO_2 interface, and significant amounts of bulk charge may also exist in the HfO_2. More detailed analyses of the V_{fb} vs. EOT relation which assume charges exist at different locations throughout the gate stack have been performed. In general, these approaches have not proven to be more successful at accurately predicting metal gate work functions. To separate out the impact of fixed charges on metal work function, additional work comparing photoemission studies with work functions extracted from the V_{fb} vs. EOT relationship should be performed. Along with the work presented in this paper there have been some recent attempts at explaining the contributions to Fermi level pinning. One recent publication proposes that oxygen vacancies in the HfO_2 contribute to the undesirable shifts of the effective metal work function.[208] Another recent paper proposes that thermal instabilities at the metal-dielectric interface induce extrinsic defects which result in undesirable effective metal work functions.[209]

In summary, a significant amount of research remains to be performed on high permittivity dielectrics, metal gate electrodes, and their interfaces. Emphasis should be placed on identifying the specific defects in HfO_2 that are responsible for charge trapping, obtaining a better fundamental understanding of how the electrode properties influence the interface stability and the effective work function, and finally, emphasis should be given to studying the physics of Fermi level pinning as it relates to the metal-HfO_2 interface.

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Vita

James Kenyon Schaeffer III was born in Owosso, MI on December 22, 1974. James is the oldest son of James Kenyon Schaeffer and Sally Lynne Schaeffer. The family has lived in Colorado since 1977. James graduated from Cherry Creek High School in Englewood, CO in 1993. After high school James enrolled at Cornell University in Ithaca, NY and graduated with a bachelors of science in Materials Science and Engineering in 1997. After graduation James accepted a job with Motorola's Semiconductor Products Sector in Austin, TX (currently Freescale Semiconductor). Work at Motorola included a year on the Engineering Rotation Program, a materials and process research position working on high permittivity embedded DRAM capacitors, and a position studying high permittivity gate dielectrics and metal gate electrodes within the Advanced Products Research and Development Laboratory. With Motorola's sponsorship, James entered graduate school at the University of Texas at Austin in August of 1999 to study Materials Science and Engineering. James joined Dr. John Ekerdt's research group to pursue the study of thin films and interfaces. James has authored or co-authored 17 papers, and is the inventor or co-inventor of 3 granted patents and 6 filed patents. James has also been an invited speaker on the topic of metal gate electrodes at the 2003 IEEE Semiconductor Interface Specialists Conference, the 2004 Materials Research Society Symposium, and the upcoming 2004 IEEE International Electron Devices Meeting.

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